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Strategic R&D Programme on Technologies for Future Experiments

Annual Report 2021

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Experimental Physics Department

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Introduction

In autumn 2017, an initiative was launched to conceive and establish a strategic R&D program on technologies for future experiments. It was initiated by the Head of the Experimental Physics department of CERN and is also referred to as the EP R&D program.

The EP R&D program is strategic in the sense that it aims at developing those key detector technologies that will be needed for the next generation of experiments. The results of these R&D activities shall be building blocks, demonstrators and prototypes. In general, the R&D does not include the development of experiment-specific final devices.

The landscape of particle physics instrumentation at the high energy frontier is well defined until the completion of the High Luminosity upgrade of the LHC (HL-LHC), scheduled for the long shutdown LS3 (currently planned from 2026 to 2028). With the full exploitation of the potential of the HL-LHC as clear top priority for the next 15 years, a number of studies for a major post-LHC project at CERN are also being pursued: FCC-ee, FCC-hh, CLIC.

The 2020 update of the European strategy for particle physics has identified an electron-positron Higgs factory as the highest-priority next collider. For the longer term, a proton-proton collider at the highest achievable energy (at least 100 TeV) is the goal, and the e^+e^- collider could be a first stage for this machine. In addition to the accelerator R&D to prove the technical and financial feasibility of this future circular collider, the European strategy update document also clearly highlights the need to keep a strong focus on instrumentation and state-of-the-art infrastructures. Instrumentation remains a key ingredient for progress in experimental high energy physics.

Throughout the years 2018 and 2019, in a series of public meetings with strong participation of external groups, the R&D workplan emerged in a process that was largely bottom-up driven. The proposals of key technologies to be pursued and further developed exceeded the expected budget envelope and prioritisation by the Steering Committee[1] was unavoidable. In addition to the scientific need, also the expertise and infrastructure available at CERN played a role in the choice of topics. A further factor to be considered was the special role that CERN plays in a number of transverse technologies like ASIC design, high-speed optical links, mechanics and detector cooling, software, and experiment magnets. Some of these technologies require continuity and a critical mass which goes beyond the size of most university groups. The result was a set of 11 work packages, where the first four are focused on different aspects of Si pixel sensors (hybrid and monolithic). One work package targets new developments in gaseous detectors and another one focuses on calorimetry and light-based detectors (such as RICH and scintillating fibre tracking). Five more work packages deal with the above-mentioned transverse technologies that will play crucial roles in any future experiment. The work program was documented in a comprehensive report[2].

The R&D program was presented in spring 2019 to the CERN Enlarged Directorate and was approved for an initial period of five years (2020-2024). The resource situation did not allow to grant, at this stage, the budget estimated for the full program. To partially compensate for this shortcoming, an arrangement was made with the four LHC experiments and the three EP support groups. They contribute about 10% of their fellow and student quota to the R&D program. In return, every R&D fellow can spend up to six months in other (non-R&D) projects of the experiment or the support group. Parts of the proposed programme were descoped or postponed.

[1] The Steering Committee has members from all large LHC experiments, the EP support groups and representatives of the above-mentioned studies.

[2] Strategic R&D Programme on Technologies for Future Experiments, December 2018, CERN-OPEN-2018-006

All work packages are open to external participants and, in many cases, the cooperation relies on structures grown over many years in detector projects. In the domains of radiation hard silicon and gaseous detectors the work packages overlap on purpose with the activities of the RD50 and RD51 collaborations, leading to synergy and flexibility.

The workplan of the R&D program foresees the major part of the work to be done by fellows and Technical or Doctoral students, while staff members spend a fraction of their time to supervise and support the fellows and students, or, as WP Leaders, to steer the research work.

This first Annual Report[3] presented in 60 pages the activities in all eleven work packages and main achievements of 2020. The fellows and students were also encouraged to play an active role in the editing process. Given the unusual, COVID-related, circumstances under which this R&D program had to take off, the wealth of activities and results underlines the outstanding motivation and effort of all participants.

In 2021, CERN launched a new Quantum Technology Initiative (QTI), which also includes some activities on quantum sensing[4]. QTI is attached to the CERN IT department, which reflects its focus on quantum computing and communication. However, strong links to EP R&D exist through two joint PhD projects on graphene-based functional structures and quantum-dot-based scintillators and nanostructures.

Summary of 2021 activities

This report summarises the main achievements of the EP R&D program in the second year (2021). Compared to the 2020 report, the volume of the report has grown to 120 pages, reflecting the increased activities and numerous results. More information can be found in presentations, notes and publications to which numerous references are included in the text.

Resource overview[5]

Towards the end of 2021, the EP R&D program reached a workforce of 27 (29) fellows and 17 (17) technical and doctoral students which comes very close to the plan (plan figures in parenthesis). The slightly lower fellow recruitment results from the persistent difficulties to find suitable candidates for certain engineering categories (ASIC design, optoelectronics). 30 staff members spend a fraction of their time as work package leader, deputy or supervisor, adding up to about 7 FTE.

The program profits from additional doctoral students who are entirely funded through the German Gentner or the Austrian PhD programs. Several EP R&D work packages have defined shared posts with the EU financed AIDAinnova Research Infrastructure project that kicked off in April 2021. Often, the AIDAinnova funds would be too small to finance a full student. The cooperation and exchange with other groups is highly beneficial for both sides.

2021 material expenditure amounted to 2.0 MCHF while 2.5 MCHF were planned. The reason for the slightly lower spending is mainly COVID-related but also due to several orders (wafer submissions) for ASICs and optoelectronics in the 50 k range which were issued in early 2022 and hence are not included in the 2021 figure.

[3] Strategic R&D Programme on Technologies for Future Experiments, Annual Report 2020, April 2021, CERN-EP-RDET-2021-001

[4] https://quantum.cern/quantum-sensing-metrology-and-materials

[5] The support in administrative and financial matters by C. Decosse and V. Nazical is greatly acknowledged.

Scientific events

An EP R&D Day took place on 14 and 15 of November 2021[6]. A full day was devoted to the review of progress and plans of the 11 work packages after almost 2 years of research activities. This was followed by a half day jointly organized with the US Electron Ion Collider (EIC) project which is in a gradual approval phase. This meeting allowed to better understand the respective needs and potential for cooperation, particularly in the domains of Silicon (monolithic) sensors, Micro Pattern Gas Detectors (MPGD), calorimetry, particle ID and electronics, as well as computing and software. The current EIC schedule foresees detector installation in the late 2020s, which is very demanding, however many technologies developed in our R&D program should be excellent stepping stones for specific EIC developments. We foresee a continuation of this exchange in 2022.

Confronted with the continuation of the COVID-related restrictions on access and live meetings, in April 2021 we introduced a monthly EP R&D internal seminar series, with the first nine seminars held online and the tenth in a hybrid format. Every seminar consist of two talks by EP R&D fellows or students about their research topics. The seminar is well received with typically 35 participants and can hopefully soon be held as a regular live event.

Some highlight achievements in 2021

As the reader will appreciate by reading through the chapters, an enormous amount of work has been performed leading to numerous remarkable achievements. A small selection of them is mentioned here as an appetizer:

Work Package 1.1, Hybrid Silicon Pixel Detectors, pushes the limits on all fronts: hit rate, speed, spatial and timing precision as well as radiation hardness. A side activity, aiming at the demonstration of the Silicon electron multiplier (SiEM), which is a new – yet to be experimentally proven - concept with intrinsic gain, attracts lots of interest. It was even granted additional funds in December 2021 through the AIDAinnova blue sky R&D call.

The work on the Monolithic Silicon Pixel Detectors (WP 1.2) in TowerJazz 65 nm CMOS Imaging Technology led in December 2020 to a so-called MLR submission to which several external groups participated, also financially. The submission included numerous chips with transistors, test structures, analog and digital pixels designs etc.. Their characterisation, in various lab set-ups, after irradiation, even in beam tests as pixel tracker, revealed excellent performance. The sensor modifications, developed and validated in the past on the 180 nm technology, are also effective in the 65 nm technology. This is a big step forward but others have to follow to assess radiation hardness and demonstrate the so-called stitching technique which allows to fabricate wafer-size CMOS sensors.

WP1.3 focuses on technologies enabling the construction of Silicon Modules. Based on dedicated lab infrastructure and expertise, a network of CERN services, external companies and institutes, WP1.3 was able to develop and characterize a whole range of impressive silicon detector modules, including multi-chip assemblies.

Work Package 1.4, which deals with the characterisation and simulation of Silicon detectors, completed the commissioning of a complex set-up called Two Photon Absorption – Transient Current Technique (TPA-TCT). The development of this set-up which had started in 2019 managed straightaway to make crucial contributions to the characterisation of the RD53B pixel sensor and charge collection studies of LGAD sensors.

[6] https://indico.cern.ch/event/1063927/

Impressive progress has been demonstrated by the work package on gas based detectors, WP2. From the numerous results the fabrication of large area PICOSEC sensors (10 x 10 cm^2) is clearly a highlight achievement and increases the range of applications such a detector may have.

WP3.1, Noble Liquid Calorimetry, has completed a large part of the study on the usability of LAr for high-granularity calorimetry in the FCC-ee and FCC-hh environments. Readout electrode studies as well as high-density feedthrough designs have been completed with success, leading to a full performance study performed in the Key4HEP software framework (WP7). The team is now extending its work plan to the construction of a demonstrator module – a task which was originally part of the work plan but removed for resource reasons. Also the very systematic R&D on scintillator based calorimetry (WP 3.2 and 3.2.1) led to a wealth of impressive results that are of highest relevance for an upgrade of the inner part of the LHCb ECAL.

WP4 – Mechanics pursues a broad spectrum of activities, from lightweight detector structures through thermal management to robotic applications in complex experimental environments. A highlight was the feasibility demonstration of an ultralight vertex detector with large (wafer scale) cylindrically-bent dummy Silicon sensors, together with a forced air flow cooling technique. These pioneering technologies are expected to be used in the ITS-3 upgrade (LS3) of the ALICE vertex detector.

The R&D on Integrated Circuit Technologies (WP5) made great progress in 2021. A first chip called TID28 was designed and fabricated in TSMC 28 nm bulk CMOS technology. The chip was found to be fully functional and its evaluation is ongoing, including first irradiation campaigns up to 1 Grad. A set of 3 more chips (the EXP28 chip set) has been submitted for TID, SEE and analog block studies. The test results will be crucial for paving the way for eventual applications at future FCC-hh experiments where radiation levels of 30 Grad in the inner tracker regions are expected (at Ldt = 30 ab^{-1}).

Furthermore, the second main activity, aiming at novel designs for efficient DC/DC converters that transfer power to the components in the heart of the detectors, made even faster than expected progress. A fully working 48V DC/DC converter, baptised bPOL48V_V2, has been successfully designed and tested.

WP6 - High speed links demonstrated radiation hard data transmission (10 MGy TID and 3 x 10^{16} 20 MeV n/cm^2 NIEL) with a Germanium photodiode to implement a 5 Gbps receiver and a modified ring modulator to produce a clean NRZ eye-diagram at 25 Gbps. The pioneering work on Silicon Photonics led to the proof of concept operation at 25 Gbps NRZ and 25 Gbps PAM-4.

Coordinated efforts in WP7 – Software to make simulation and analysis in future experiments faster and more efficient have led to a number of great results. The initial RNTuple performance measurements show that it beats all other formats, both the current ROOT TTree and non-HEP data science formats for size on disk and read speed. Equally impressive are the results using meta-learning to develop generative ML models that rapidly re-train themselves for different calorimeters

The Detector Magnet R&D, WP8, pursues a set of studies with shorter and longer term goals. An example is the construction and integration of a full snubber (damper) circuit in the ATLAS Toroid system. Once commissioned in 2022, it should capture voltage spikes and related arcing and discharges. The design study of a 4T magnet test facility advanced last year to a state which allowed to various concepts to be compared, finally favouring a Split Coil Solenoid design.

Outlook

From a resource point of view, 2022 will be a peak year, with total resources increasing by about 20% compared to 2021. The first generation of fellows will be in their 3rd year and we will profit from their

increased autonomy and accumulated expertise. The R&D activities should continue, close to the initial plan, and generate plenty of results. In 2022, we foresee two EP R&D Days. One, in early summer, that will review the status of all work packages and compare them with the original list of milestones and deliverables defined in 2019. This will also be the occasion to have a systematic look at the 2021 ECFA Detector R&D Roadmap and discuss possible adaptations of the EP R&D plan which will by then be 5 years old.

The initial funding period from 2020 to 2024 was always considered only as the start of a continuous and long term R&D program. A second EP R&D day is envisaged for late 2022 and should be the right moment to discuss and agree on a 5-year forward projection of the EP R&D work plan for the years 2024 – 2028. The programme update shall be in line with the ECFA roadmap program but also with CERN's specific needs and priorities. This process will also lead to a new budget estimate to be included in the CERN Medium Term Plan exercise in spring 2023.

WP1.1 Hybrid Silicon Pixel Detectors

1. Introduction

WP 1.1 focuses on hybrid silicon sensors for charged particle detection. It targets intensity frontier applications that require specialized sensor and/or complex ASIC features: high fluence (>$10^{16}n_{eq}/cm^2$), high hit rate O (10 Ghits/s/cm^2) and/or high output bandwidth O (100 Gb/s) with spatial resolution below 10 µm and temporal resolution below 50 ps. The work plan is articulated around four axes: the development of sensors matching the targeted resolutions under the fluences discussed above as well as their characterisation pre- and post-irradiation; the development of simulation tools allowing to understand the sensor characteristics and to aid the design process; the development of a fast timing and high rate telescope based on the Timepix4 ASIC to both characterise sensors and study system level timing; and the design of integrated electronics capable of handling the sensor signals at high rate. The WP work plan is tightly linked to the work done in the WP 1.2, 1.4 and 5, as well as with other R&D initiatives such as RD50, AIDA-innova (Timepix4 planes for EUDET telescope, iLGAD production, SiEM production), other institutes' R&D (collaboration with Nikhef, CPPM, USC, University of Oxford,...) and CERN experiment upgrades (LHCb, NA62). A senior fellow and a doctoral student joined the WP in 2020 and were joined this year by a senior fellow who will work in 2022 on ASIC design for silicon pixel sensor front-end. During the first 6 month of his contract the fellow worked for EP-ESE on the design of Medipix4 in view of its submission the 21st March 2022. The WP also hosted two summer students and a technical student for 3 months on the design of the cooling plate for the Timepix 4 telescope.

2. Main activities and achievements in 2021

2.1 Sensor production and characterisation

The production of n-in-p planar sensor wafers which was prepared in 2020 was realised in 2021 by ADVACAM. It features several sensor geometries (Timepix4, Timepix3 and TDCpix) as well as a set of structures for R&D. Those sensors and structures were produced in various thicknesses (50, 100, 200 and 300 µm) as this parameter is expected to be crucial for time resolution and radiation hardness. While the large scale sensors, once bonded to readout ASICs, allow to investigate the global timing performances of the hybrid sensors, the test structures were produced in order to conduct an extensive study of the timing properties of planar technology as function of sensor thickness and integrated fluence, as well as to provide benchmarks to test simulation tools discussed in section 2.2. A first batch of four sensors were bonded to Timepix4 v1 ASIC. After dicing of the sensors, large bow were observed on the individual die (up to 90 µm for the 100 µm thickness sensors). Bump-bonding was nonetheless possible and the resulting hybrid showed good flatness as illustrated in Figure 1a.

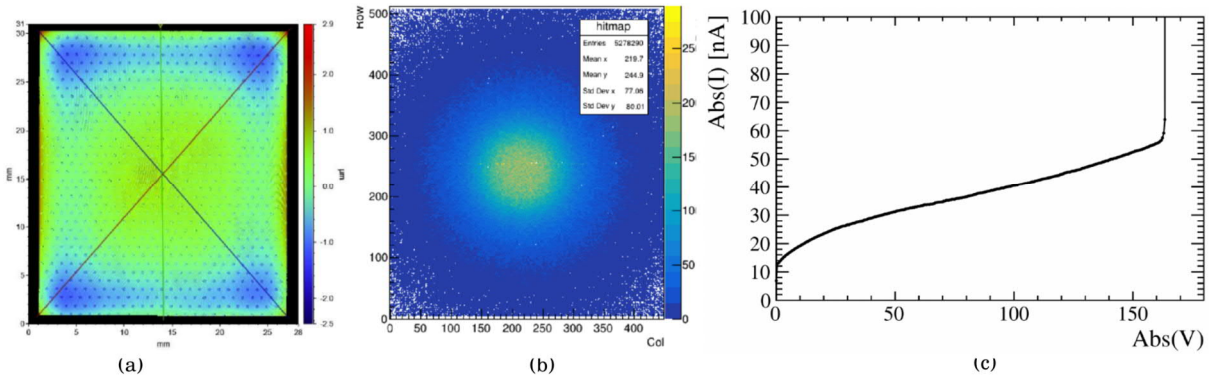


Figure 1: Profile of the 100 µm sensor once bonded to a Timepix4 ASIC (a); Hit map of the sensor when exposed to a Sr90 source (b); I-V characteristic curve of a 300 µm Timepix4 assembly (c).

First tests with Timepix4 readout and radioactive source were performed at Nikhef and the sensors were used for the first run of the Timepix4 telescope. The overall performances are good, with depletion voltage ranging from a few volts for the 50 µm sensors to 50 V for the 300 µm sensors. More sensors will be bonded in 2022 to Timepix4 v2, both for sensor studies and to equip the second arm of the Timepix4 telescope, while TDCpix footprint sensors will be bonded to TDCpix ASICs for NA62 upgrade studies. In Figure 1c, the IV curve shows that the breakdown voltage happens around 150 V which for the thicker sensor does not allow to reach the electron saturation velocity. This effect is studied further with the test structure. The R&D test structures consist of several 3 and 1 mm wide diodes, 5x5 pixel matrices with a pixel pitch of 55um and structures for secondary ion mass spectroscopy measurements. The characteristics of the R&D test structures were measured before irradiation. In particular CV and IV measurements were done at the IV setup of the RD50 collaboration. As for the full sensors, the measurements showed an earlier than expected breakdown, which was further studied using simulations, and is discussed in section 2.2. Characterisation of the charge collection and time resolution is on-going with the source setup described in section 2.3.

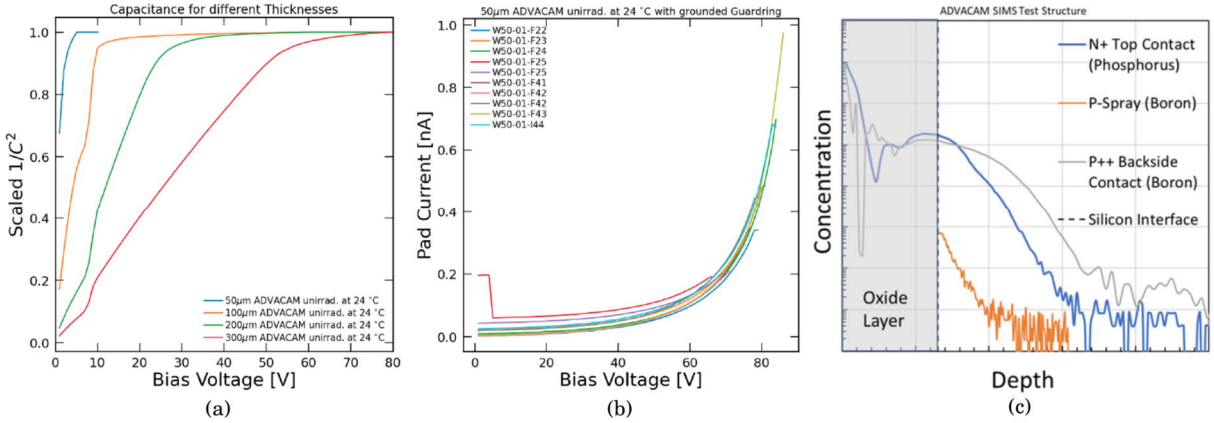


Figure 2: CV measurements of the 3 mm diode at 1000 Hz scaled to the capacitance value after depletion for different thicknesses. The structure at around 10V present at all thickness is due to the lateral depletion of the region close to the interface between the n+ implant and the p-spray (a); IV measurements of 50um thick 3mm diode test structures (b); Doping Profiles for the different test structure implants as measured with SIMS (c).

In order to perform an accurate simulation of the test structure performance before and after irradiation, the exact knowledge of the doping profiles is required. In the context of a non-disclosure agreement signed with ADVACAM, the doping profile will be evaluated with process simulations while it was also measured though Secondary Ion Mass Spectroscopy (SiMS) performed at the Groupe d'Etude de la Matière Condensée in Versailles. The analysis of this measured data allowed for a precise resolution of the profile of the different implants, illustrated in Figure 2. A resolution of 10^{15} atoms/cm for the n- implant concentration of $4.5x10^{14}$ atoms/cm for p-spray concentration has been achieved. An irradiation campaign is currently ongoing. For each of the 10^{15}, $8x10^{15}$, $6x10^{16}$ and 10^{17} 1 MeV n_{eq}/cm^2 fluences, IV, charge collection efficiency and time resolution will be measured to characterise the structures. Neutron irradiation campaign at the TRIGA reactor at Ljubljana will be finished by March 2022 while proton irradiation is planned at IRRAD at CERN, from April to Nov. 2022.

In the LGAD radiation hardness studies presented in 2020 [1] and 2021 [2,3], a 20 % improvement in charge collection was established for deep carbonated substrates without noticeable effect on gain layer deactivation. Expanding on these results, the level and placement of carbon implants was studied. The gain layer dopant distribution and carbon content of FBK and CNM produced LGADs was characterised through a combination of SIMS measurements and TCAD process simulations. Resolutions of $(1.35 \pm 0.58) \times 10^{14}$ and $(4.71 \pm 0.03) \times 10^{16}$ atoms/cm^3 were achieved for boron and carbon concentrations, with depth uncertainties < 10 µm [4]. The obtained profiles shown in Figure 3, reveal fundamental differences between the deep carbon implant approach, resulting in a lower and

more uniform concentration as function of depth (Fig. 3a), versus the approach of a carbon implant at gain layer level (Fig. 3c). The first acts at a substrate level, reducing trapping for high resistivity p-types, while the second acts by decreasing boron deactivation through acceptor removal. A combination of both processes is now considered for upcoming LGAD productions to further extend radiation tolerance.

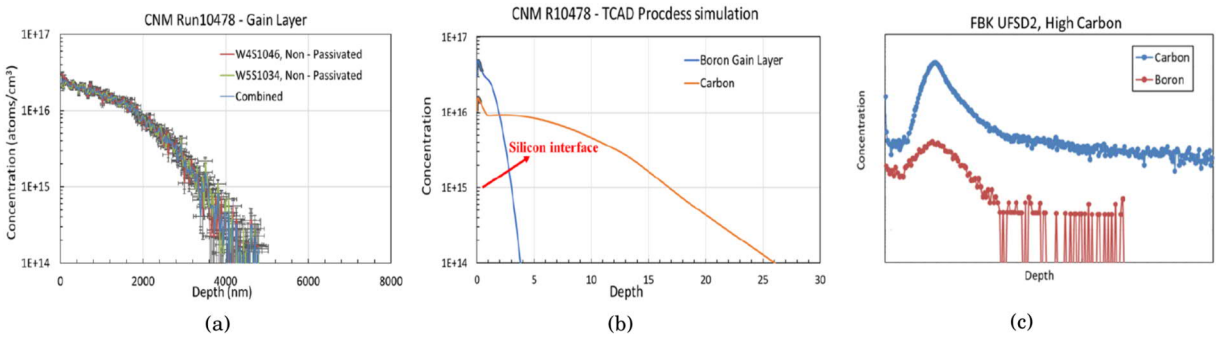
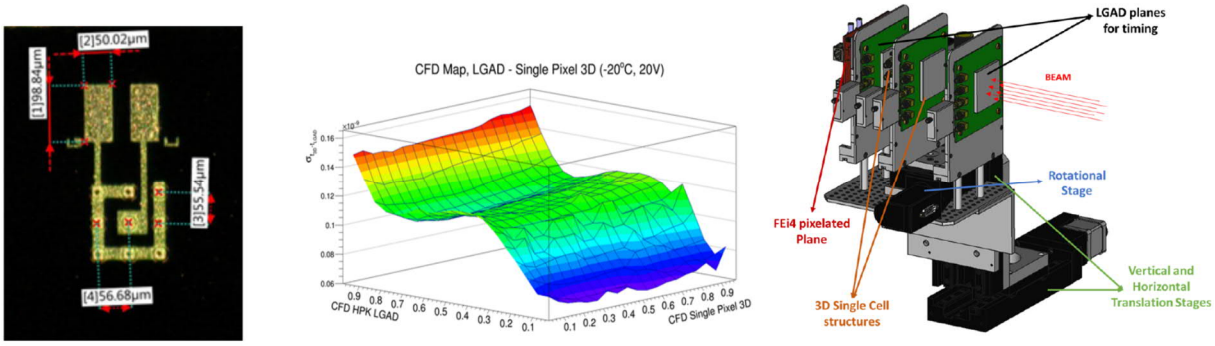


Figure 3: SiMS measured boron gain layer profile (a) and TCAD simulated Carbon and boron profiles (b) for CNM deep carbonated process. An agreement of 5% level between measurements and simulations is observed. SiMS measured boron and Carbon profiles for the gain layer level carbon implantation (c) of FBK samples. Axes are omitted for confidentiality purposes.

The choice of alternative implants for defect engineering was also examined. The case of Indium for formation of the gain layer was studied in detail [5] while Lithium co-implantation is suggested. The latter can act in one hand as gain layer compensation, allowing for higher acceptor concentrations in unirradiated structures. Indium additionally provides the potential for beneficial defect engineering. As a result of this study, an RD50 common project request was approved for further investigation (project RD50-2021-03). The simulations and mask design for this test-run has been completed but shortages in the global wafer market and fabrication related delays have pushed the expected arrival date of first samples towards the 3rd trimester of 2022.

Similarly, the production of pixelated iLGADs wafers, to which the WP participates through a RD50 project, which was planned for the second half of 2021 have been delayed and is only expected during 2022. It features the same full sensor footprints as the planar production which will allow easy benchmarking. The aim of the iLGAD technology is to improve the fill-factor with respect to traditional LGADs by implementing the multiplication layer on the backside of the sensor, making it independent of the readout segmentation [6].

3D sensors have proven their potential to operate at radiation fluences much higher than 10^{16} n_{eq}/cm^2, while achieving pitches of ~50 µm with <100 psec time resolution. Such characteristics make the technology an excellent candidate for 4D tracking applications. As a case study, the time resolution of a single 120 x 120 μm^2 3D pixel cell (Fig. 4a), was studied through β-source charge collection measurements at various temperatures. The standard deviation of the time difference between the reference LGAD plane and the 3D cell for various thresholds is presented in Fig 4b [7]. As expected, the 3D time resolution is independent of the applied threshold and a value in the order of 40 ps was measured. To evaluate the variation of the time resolution as function of the particle incidence angle, a test beam campaign was devised using 160 GeV SPS pions. A combination of LGADs and a pixelated matrix formed a timing telescope shown on Figure 4c, allowing for precise timing measurements at angles varying between +/- 12º. In a second campaign, the timing telescope was integrated within a MIMOSA tracking telescope in order to establish a detailed sub-pixel timing map. While the analysis of the two campaigns is ongoing, preliminary results demonstrate a spatial resolution of 3-5 µm. Identically to the planar production, several structures were irradiated and will be tested during 2022. Test beam campaigns are performed in collaboration with members from IFAE, IGFAE and ATLAS AFP.

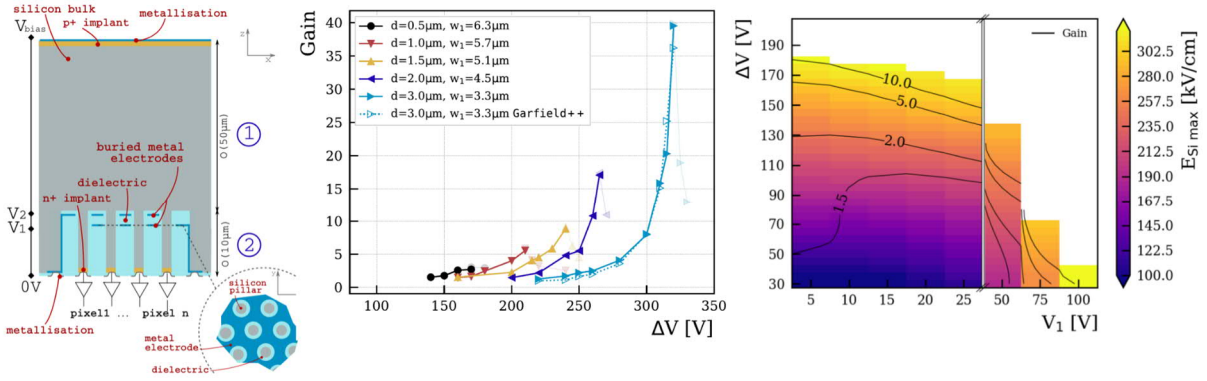


(a) (b) (c)

Figure 4: Top view of a single 120 x120 µm² pixel with 55 µm column distance (a). Time resolution of the LGAD-3D system with respect to the CFD threshold applied at each sensor (b). A 3D model of the timing telescope with 2 LGAD planes as timing references and a pixelated plane for alignment, integrated with a three axis motion system (c).

Early simulation in 2020 showed that primary charge amplification could be achieved with a new concept of sensor with intrinsic gain, the Silicon electron multiplier (SiEM). The principle of this sensor is illustrated in Figure 5a.

The expected performances of the Silicon electron multiplier (SiEM), which is a new concept of sensor with intrinsic gain, were studied this year with TCAD simulation. In this sensor the internal gain is not achieved through doping, as in LGADs, but by burying electrode grids into the semiconductor substrate as illustrated in Figure 5a. A full description of the concept can be found in [8]. The aim is to achieve good timing performances thanks to the internal gain but without suffering the radiation sensitivity observed in LGADs. Early simulation in 2020 showed that amplification could be achieved. In 2021 the impact of the pillar and electrodes geometry as well as the biassing scheme on the behaviour of the structure were studied.



(a) (b) (c)

Figure 5 : A cross section and top view of the Silicon Electron Multiplier (a); Gain as function of ΔV for various inter-electrode distance (b); Gain and maximum electric field in the silicon for various biassing scheme (ΔV= V_2-V_1) (c)

Adjustment of the geometry allows to optimise the sensor performance, but also to find parameters that permit it to achieve amplification while remaining far from breakdown. For instance, variations of pillar height, electrode widths and pitch has been simulated. Examples of those studies, which are reported in details in [8], are given in Figure 5. For a structure with 2 µm wide pillar with pitches of 10 µm, Figure 5b shows how the gain evolves as a function of the difference of voltage between the two amplification electrodes, ΔV. It is displayed for different inter-electrode distances. With the higher distances, high gain can be achieved with low fields in the silicon oxide. The biassing scheme of the device also gives a way to mitigate the field in the silicon and in the dielectric. By default, large ΔV were envisaged to achieve amplification, but the high field is better spread in the pillar by sharing the difference of potential between ΔV and V_1, the difference of potential between the readout electrode and the first amplification electrode. This is illustrated in Figure 5c that reports the gain and maximum

field in the silicon as function of V_1 and ΔV. The next step is to make a demonstrator for this sensor and for this two paths are followed. The original envisaged fabrication scheme is based on deep reactive ion etching followed but successive metal and dielectric deposition. A collaboration was setup with CNM-CSIC to develop this fabrication process and was granted funds in December 2021 through the AIDAinnova blue sky R&D call. In parallel, another approach is investigated together with a team of the Paul Scherrer Institute and is based on metal assisted chemical etching [9], a more prospective technology for those applications. The advantage of this technology is that the catalyst used for the etching can be used as a seed for the electrode metalization, relaxing some of the constraints with respect to the DRIE based process. The work on both projects will start at the beginning of 2022.

2.2 Sensor simulation

Device simulations of planar test structures were done to understand the measured characteristic of the sensors discussed in 2.1 before irradiation. A 2D model of the small test structures was constructed in Sentaurus TCAD and different mesh sizes were tested to find a good compromise between simulation time and precision. The cause of the early breakdown observed in the IV measurements was identified as due to the high p-spray doping concentration leading to impact ionisation in the interface region between the interface of the implant of the readout electrode/guard ring and the p-spray, Figure 3b. CV simulation shown in Figure 6a, also helped to explain the additional step seen in Figure 2a, which originates from the extension of the depleted region in the pn-junction between the p-spray implant and the electrode implant.

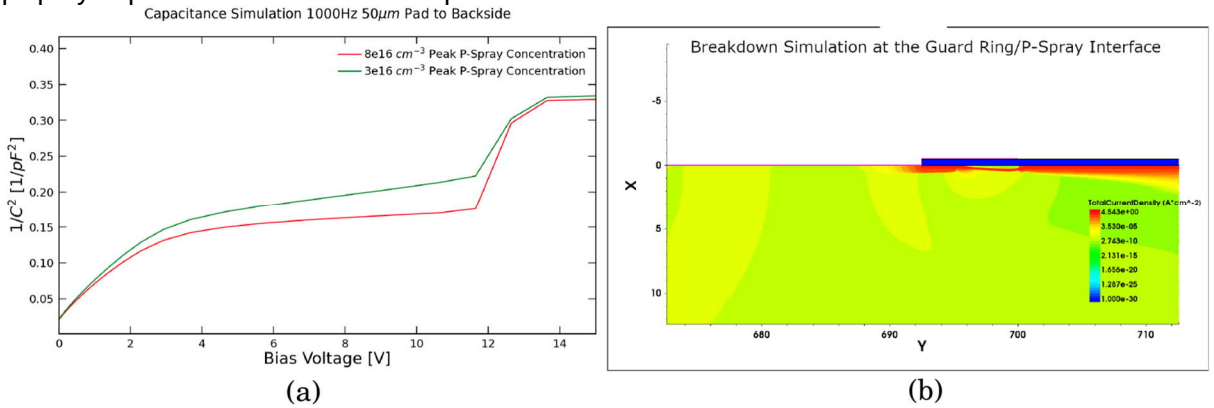


Figure 6:CV simulation of test structures for different peak concentrations of the p-spray (a). 2D simulation of the current flow during breakdown at the guard ring/p-spray interface (b).

With the upcoming measurements of the irradiated sensors, commonly used radiation damage models will be tested in TCAD to allow the comparison of IV, CV and timing simulation of irradiated planar sensors to the data.

Simulation of the signal time structure in planar pad and pixel detectors were performed by a summer student with Garfield++. The outcome of this work is summarised in [10] and shows the impact of parameters like the choice of shaper, sensor thickness, noise and temperature on the hybrid time resolution. Garfield++ simulations were also used to simulate sensors with internal gain. Comparison of the gains obtained by TCAD transient simulations of the SiEM to those obtained by Garfield++ shows agreement within 5%, as illustrated in Figure 5b. The detailed Monte-Carlo charge transport simulations done with Garefield++ will allow to evaluate the expected time response of the SiEM to minimum ionising particles.

2.3 Fast telescope and other timing setups

Discrete readout electronics with two stage amplification is used for the studies of test structures. Up to now most of the setups used by the WP were based on a board developed by UCSC for LGADs. Because LGADs signal have a “slow” rise time, the pre-amplifier was optimised for a signal frequency below 1 GHz. For both 3D and planar studies this is no longer sufficient and a dedicated 16-channel

board integrating a dual stage amplifier design with a uniform response up to a frequency range of 8 GHz was developed (Fig. 7a). A single SiGe transistor configuration is used for both stages, with the first acting as a transimpedance amplifier and the second as a voltage amplification stage. The design features a passive daughter board for versatile sensor replacement, triaxial HV input and coaxial outputs, implemented on a hermetically EM shielded HF-Rogers dielectric (Fig. 7b). Preliminary tests indicate a total gain of 70 with both stages combined and an SNR of 28 for a typical 50 µm planar pixel sensor signal [7]. More tests are underway to evaluate inter-channel cross-talk with a 4x4 100 µm thick pixelated matrix.

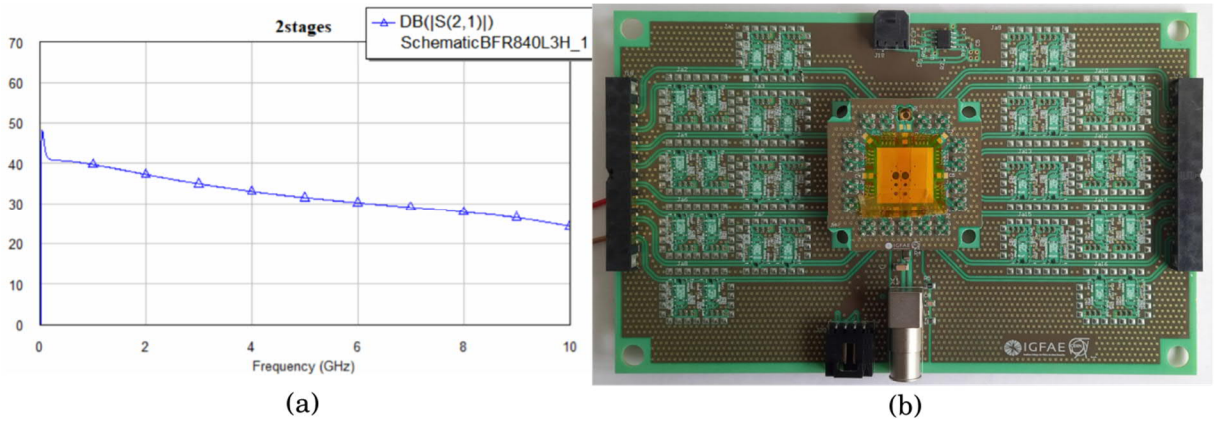


Figure 7: Simulated Gain (dB) vs Frequency response of the complete two stage amplification chain (a). First prototype of the 16-channel board with the accompanying sensor daughterboard attached (b). The HV and temperature monitoring connectors are visible at the front with the signal outputs on both lateral sides.

The WP 1.1 is involved in the construction of a charge particle telescope based on Timepix4 ASIC targeting spatial resolution down to 2 µm, track time stamping capabilities with time resolution down to O(30ps) and high readout rate capabilities allowing to exploit the full SPS rate. It is based on Timepix4 readout and is a collaboration between CERN, Nikhef, USC, the University of Dortmund, the University of Oxford, IFCA and the University of Manchester. The CERN group designed the mechanics for the telescope support and arms and the DUT box with vacuum and cooling capacities. It implemented the motion system for the telescope and for the DUTs. The design of the 3D printed titanium cooling plate was the topic of a technical student project. Cold water is flowing through the hollow cooling plate and allows to maintain a low and stable temperature for the operation of the ASICs. In October 2021 a first testbeam campain was organised to commission the telescope.

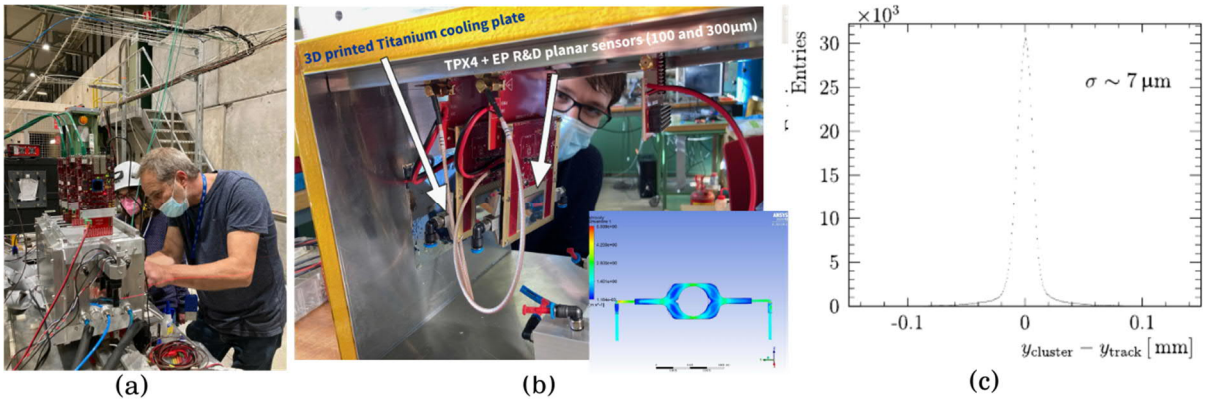


Figure 8: View of the enclosure containing one of the TPX4 telescope arm (a). Inside view of the enclosure with the TPX4 planes mounted on 3D printed titanium cooling plate and the simulated water flow inside the cooling plate (b). Residuals between the position of 3-hit tracks extrapolation and the measured clusters in the 300 µm thick sensors -from [11] (c)

The CERN group produced the mechanical part for one arm and the bump bonded sensor (see section 2.1). Fig 8 shows the setup. This first campaign was targeting commissioning of the mechanics, motion system, slow control and readout system, and as such the telescope was not equipped to achieve the

target spatial and time resolution. Nonetheless, even with only 2 thin (100 µm) and 2 thick (300 µm) sensors installed, the track residuals with respect to the recorded clusters, shown in Figure 8c, and the time resolution of the sensors, using a set of three scintillators to provide time reference, could be estimated. A paper reporting those results is under preparation and first results were shown at the Medipix meeting in Prague in November 2021 [11].

2.4 IC block design

The WP 5 is developing the key blocks needed to design ASIC in 28nm. In 2021 a fellow was hired in by the WP1.1 to develop the block specific to fast silicon hybrid sensor front-end. A collaboration with EPFL has started with the investigation of different comparator topologies using TSMC 28 nm technology. This research will determine which topology provides the best timing performances for a given power consumption and will later be implemented in the analog pixel for fast silicon pixel sensor ASIC. The fellow started studies of a charge sensitive amplifier for the analog front end. The envisaged topology uses a Krummenacher amplifier that includes a DC leakage compensation network and if its implementation of 65 nm technology is well understood, the scaling down to 28 nm requires new strategies to understand how high-performance analog blocks can be implemented.

3. Publications and contributions to conferences and workshops

Conferences:

- E. L. Gkougkousis, Comprehensive technology study of radiation hard LGADs, TIPP 2021
- V. Coco, The Silicon electron multiplier, 2021 IEEE NSS MIC

Workshops:

- 16th "Trento" Workshop on Advanced Silicon Radiation Detectors
  - E. L. Gkougkousis, Data-Driven LGAD mortality studies
  - E. L. Gkougkousis, Parametric process optimization for Indium, Gallium and Boron dopants using TCAD simulation modelling
- 12th workshop on picosecond timing detectors for Physics
  - E. L. Gkougkousis, A Comparative Study of LGAD Radiation Damage Mechanisms
- 39th RD50 Workshop
  - Halvorsen, M. M., Solid State Electron Multiplier

Publication:

- M. M. Halvorsen, et. al., "The Silicon Electron Multiplier Sensor", arXiv:2203.01036 (submitted to NIM A)

References

[1] E. - L. Gkougkousis, "Acceptor removal and gain Reduction in proton and neutron irradiated LGAD"s, CERN, 2020, 36th RD50 Workshop, Geneva

[2] E. - L. Gkougkousis, "Comprehensive Technology Study of Radiation Hard LGADs", CERN, 2021, 5th Technology and Instrumentation in Particle Physics, Vancouver

[3] E. - L. Gkougkousis, "A Comparative Study of LGAD Radiation Damage Mechanisms", CERN, 2021, 12th workshop on picosecond timing detectors for Physics, Zurich

[4] E. - L. Gkougkousis, "Detailed process characterization of carbonated LGADs through Secondary Ion Mass Spectroscopy", CERN, 2022, 17th "Trento" Workshop on Advanced Silicon Radiation Detectors, Freiburg

[5] E. - L. Gkougkousis, "Parametric process optimization for Indium, Gallium and Boron dopants using TCAD simulation modelling", CERN, 2021, 16th "Trento" Workshop on Advanced Silicon Radiation Detectors, Trento

[6] E. Curras et. al. "Inverse Low Gain Avalanche Detectors (iLGADs) for precise tracking and timing applications", NIM A, Volume 958, 162545 (2020)
[7] E. - L. Gkougkousis, "Single cell 3D timing: Time resolution assessment and Landau contribution evaluation via test-beam and laboratory measurements", CERN, 2022, 17th "Trento" Workshop on Advanced Silicon Radiation Detectors, Freiburg
[8] M. M. Halvorsen, et. al., "The Silicon Electron Multiplier Sensor", arXiv:2203.01036
[9] L. Romano et al;"High-aspect-ratio grating microfabrication by platinum-assisted chemical etching and gold electroplating", AdEM 22 (2020) 2000258
[10] De Sousa Ataide Da Silva, R.,"Time Resolution Study using Garfield++", Oct 2021, CERN-STUDENTS-Note-2021-208
[11] Van Beuzekom, M., "First tracks through Timepix4v1 beam telescope at CERN", Medipix meeting, Prague, Nov 2021

WP1.2 Monolithic Silicon Pixel Detectors

1. Introduction

Monolithic pixel sensors receive increased interest due to their potential for tracking, timing, and even calorimetry in future high energy physics experiments. The EP R&D Work package for the monolithic CMOS Pixel sensors aims to develop these sensors for future experiments in sub-100nm CMOS processes, where several applications are likely to use the same advanced technologies. Significant experience exists in the 180nm TowerJazz CMOS imaging technology with large scale production of ALPIDE [1] for the ALICE ITS2 upgrade (>10 m^2), process modifications for accelerated charge collection and radiation tolerance [2-6] applied for several experiments, in the EU funded STREAM and FASTPIX projects and several submissions with strong contributions from external groups. The TPSCo 65 nm ISC technology, the 65 nm CMOS imaging flavor of TPSCo, a joint venture between TowerJazz and Panasonic, is the first technology identified. After the first MLR submission in December 2020 and subsequent measurements it is now adopted for the ALICE upgrade of the inner layers of its Inner Tracker System (ITS3).

Five fellows, one postdoc and five Ph.D. students are active in this work package, several directly financed by EP R&D, some have been made available by the former LCD group in the early stages, three by ALICE, contributing also very significantly to the testing of the TPSCo 65 nm ISC. A significant testing effort with staff, fellows and students, also continues to be provided by groups and institutes interested in the 180 nm technology, including the DT and ADE groups at CERN. Synergies exist with several other work packages, for instance with WP1.4 for the development of test systems and simulation tools. Several activities are included in the AIDAinnova project.

Many groups inside and outside of ALICE have contributed, also financially, to the MLR submission, and also to the measurements and their preparation.

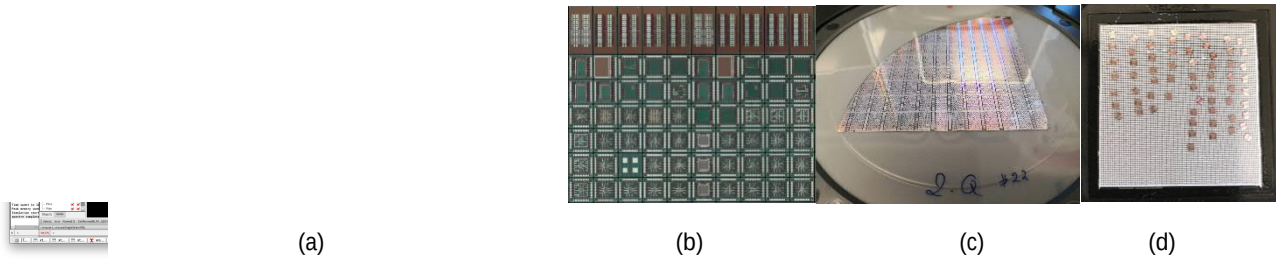
- University and INFN Torino: F. Benotto, S. Beole, C. Ferrero, V. Sarritzu, U. Savino, S. Perciballi, F. Prino, A. Turcato
- University and INFN Bari: G. De Robertis, F.Loddo
- Universi and INFN Catania: P. La Rocca, A. Triffiro
- University and INFN Cagliari: D. Marras, G. Usai, S. Siddhanta
- University of Salerno: R. Ricci
- University and INFN Trieste: M. Buckland, G. Contin
- IPHC: J. Baudot, A. Besson, R. Bugiel, S. Bugiel, C. Colledani, A. Dorokhov, Z. El Bitar, M. Goffe, C. Hu, K. Jaaskelainen, F. Morel, H. Pham, S. Senyukov, I. Valin, M. Winter (now with Orsay), Y. Wu (also with USTC)
- NIKHEF: R. Russo, V. Gromov, D. Gajanana, A. Yelkenci, A. Grelli, R. Kluit, J. Sonneveld, A. Vitkovskiy
- Heidelberg University: H.K. Soltveit, P. Becht, A. Yuncu
- Prague University: A. Isakov, F. Krizek
- Technische Universität München: L. Lautner
- DESY: A. Chauhan, D.-V. Berlea, M. Del Rio Viera, D. Eckstein, F. Feindt, I. Gregor, K. Hansen, L. Huth, B. Mulyanto, C. Reckleben, S. Ruiz Daza, P. Schütze, A. Simancas, S. Spannagel, M. Stanitzki, A. Velyka, G. Vignola, H. Wennlöf
- STFC (RAL): A. Hodges, S. Matthew, I. Sedgwick
- Oxford University: D.Bortoletto, F.Windischofer (also CERN)
- Birmingham University: L. Gonella, P. Allport
- Bolu University: K. Oyulmaz
- Zagreb University: T. Suligoj

- Yonsei University: Y. Kwon, G.H. Hong
- EPFL: E. Charbon

2. Main activities and achievements in 2021

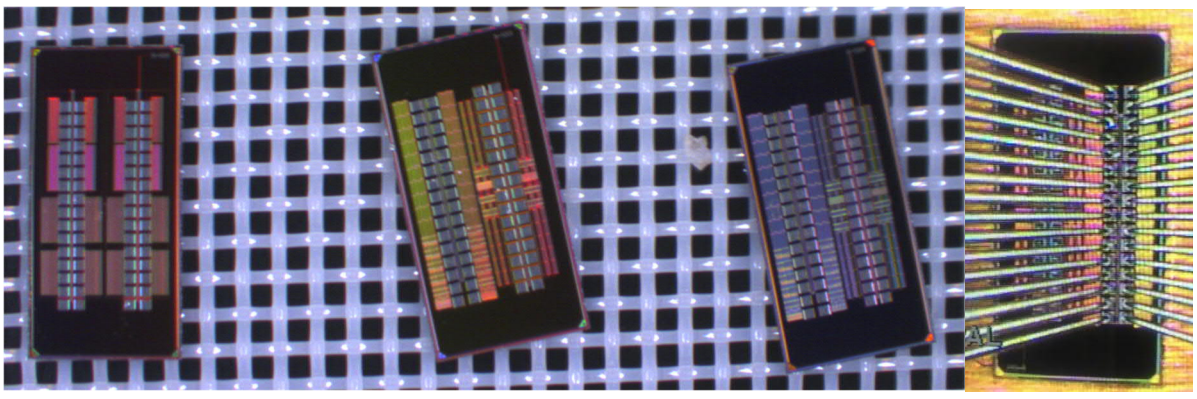
2.1 TPSCo 65 nm ISC evaluation and validation on the first MLR submission

A first submission was done as a Multi Layer Reticle (MLR), where several masks are implemented on the same reticle to reduce the number of reticles and the cost. Masks for the first MLR submission in the TPSCo 65nm ISC were approved end of 2020, with intense sensor design and process optimization continuing into January 2021 with direct regular contact with the foundry in Japan. Wafers arrived early summer, thinned and diced chips became available for testing early September. Very intense test setup developments and improvement are still in progress. The submission was in synergy with the ALICE experiment for the development of the ITS3 stitched sensor, with test chips provided by groups in and outside ALICE: CPPM, DESY, IPHC, NIKHEF, STFC (RAL), Yonsei University (South Korea). Fig. 1. shows a screenshot of the submitted designs, wafers and diced chips. They include multiple pixel test matrices, LVDS/CML receiver/driver, bandgaps, temperature sensors (T-sensors), Voltage Controlled Oscillators (VCO), amplifiers, ring-oscillators, transistor test structures as well as a interconnect test structure.



(a) (b) (c) (d)

Fig. 1. MLR submission in the TPSCo 65 nm ISC technology: (a) Layout overview, (b) one reticle field on the wafer containing 70 test chips of 1.5 mm x 1.5 mm or 3 mm x 1.5 mm (55 different ones, with 15 chips printed twice), (c) a diced quarter wafer on tape, and (d) hand picked die in a gelpack.



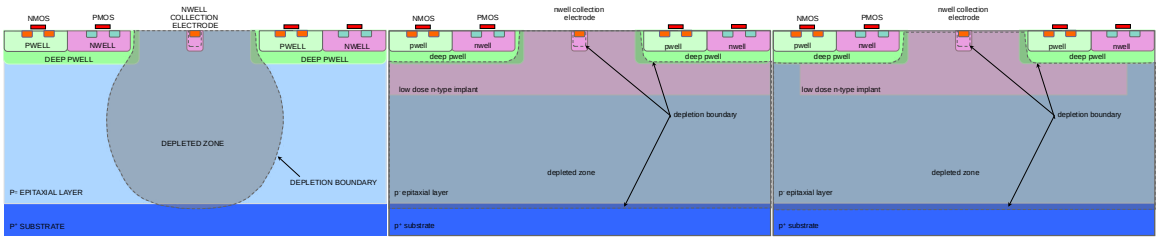
(a) (b)

Fig. 2. (a) Transistor test chips and (b) one chip under probe test.

Design kit access for the TPSCo 65 nm was granted for several participating groups and a close contact with the foundry was established, first with Israel, then directly with Japan. The participating groups

signed a new Non-Disclosure Agreement (NDA) with the foundry and several new groups expressed interest to join.

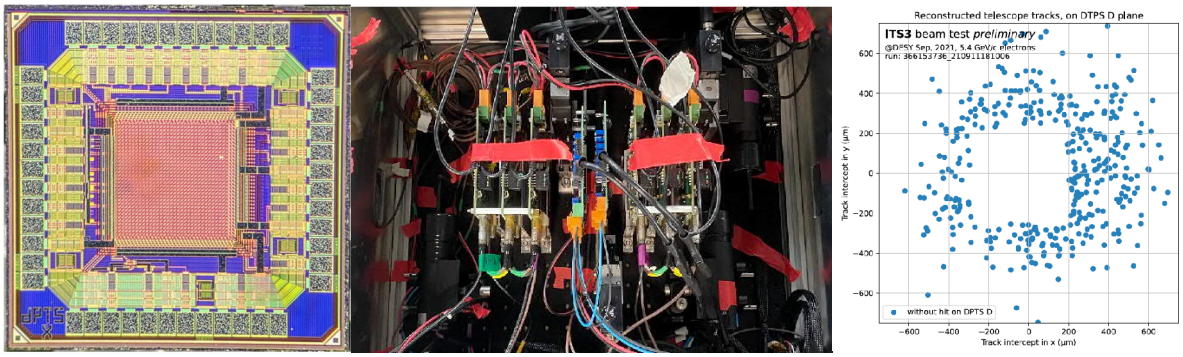
Fig. 2 shows some transistor test chips and one chip under test on the probe station. Transistor measurements indicated no major issues on any of the various transistor types.



(a) (b) (c)

Fig. 3. Various sensor designs (a) conventional, (b) modified with blanket deep low dose implant over the full pixel area (c) with gap in the same implant over the pixel boundary.

Three different pixel sensor designs (fig. 3), first validated in 180 nm, were prototyped in the first MLR run in the 65 nm ISC technology: (a) a conventional design ("standard") for which the high resistivity epitaxial layer is typically not fully depleted if a significant fraction of the pixel area is occupied by circuitry, (b) a modified one ("modified") with a blanket deep low dose n-type implant over the full pixel area to obtain depletion of the epitaxial layer over the full pixel area, and (c) ("gap") with the same implant but with a gap in the implant over the pixel boundary to enhance the lateral field and accelerate the signal charge towards the collection electrode. The designs were implemented in four process splits, one with the standard process, one with modifications to optimize especially the pixels with the additional low dose deep n-type implant, and two intermediate splits for debugging purposes.

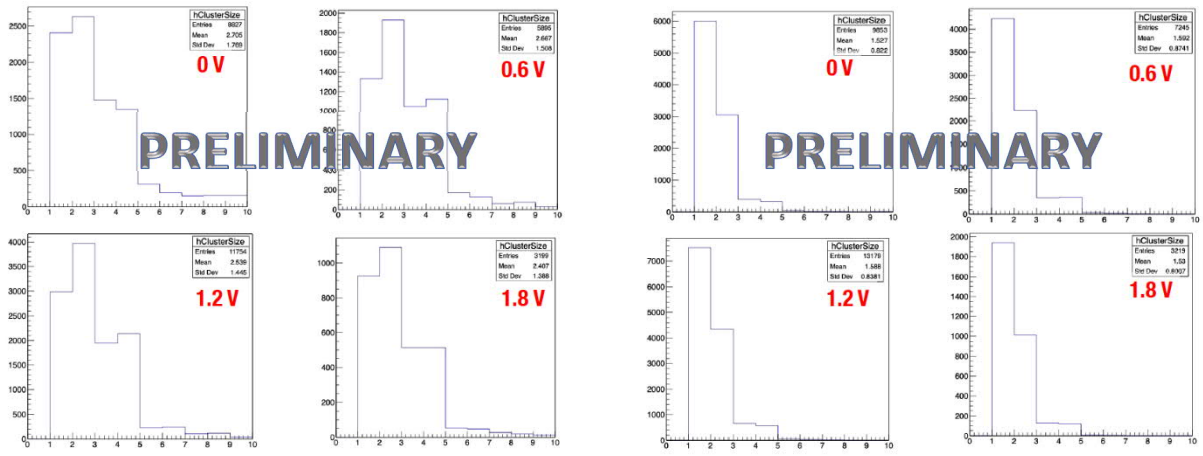


(a) (b) (c)

Fig. 4. [7] (a) Die picture of the Digital Pixel Test Structure or DPTS, (b) the ALICE test beam setup with 6 ALPIDE reference planes and 2 DPTS planes in the center, and (c) particle tracks not detected by the DPTS showing a clear 100 % shadow corresponding to the sensitive area of DPTS and illustrating the 100 % detection efficiency of the DPTS.

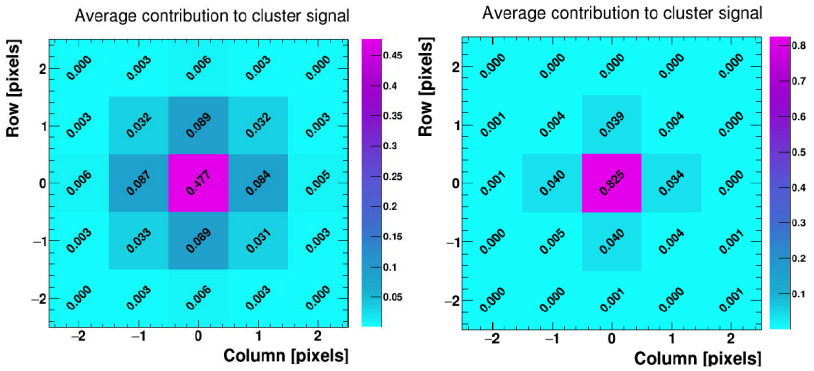
Measurements on the Digital Pixel Test Structure or DPTS (fig. 4) with sensor with gap in the optimized process split proved full detection efficiency in a test beam a few weeks after diced chips became available [7,8]. This result validated the process modification for better charge collection, and full functionality of the front end and of the digital logic. The DPTS is the most ambitious chip submitted in MLR1, it measures 1.5 mm x 1.5 mm, contains a 32 x 32 pixel matrix of 15 micron pitch, and provides asynchronous digital readout with Time-over-Threshold (TOT) information. SEU register cross-sections were also measured to be in the expected range. The foundry made a new metal stack available with more metals for power routing to reduce resistive drops and also give more flexibility in the routing of signals, and a new process design kit, digital design kit and I/O libraries were provided in a very timely

manner for the next submission. The proven front end on the DPTS is being adapted for use in the stitched sensors on the next engineering run.



(a) (b)

Fig. 5. Comparison between a conventional sensor in the standard process and a sensor with low dose n-type implant with gap measured on the APTS with source follower and 15 µm pixel pitch in a test beam at the CERN PS for different reverse substrate biases: cluster size for (a) standard and (b) gap. As expected the addition of the low dose n-type implant with gap clearly reduces charge sharing and hence cluster size.



(a) (b)

Fig. 6. Comparison between a conventional sensor in the standard process and a sensor with low dose n-type implant with gap: on CE65 [9] cluster size and seed signal contribution exposed to a ^{55}Fe source for (a) standard and (b) gap. Also here the addition of the low dose n-type implant clearly reduces charge sharing and cluster size, but also concentrates significantly more charge on the seed pixel enhancing operating margin.

Other pixel test structures, the Analog Pixel Test Structure or APTS, a chip with a 4x4 pixel matrix with analog outputs buffered to individual pads, and the CE65, designed by IPHC, containing a 64 x 32 pixel matrix at 15 µm pitch with rolling shutter readout are implemented in many variants to study the pixel sensor performance for different pixel designs and process splits. Groups from the ALICE collaboration, CERN and other institutes, in particular the INFN with Cagliari, Catania, Torino and Trieste, and also NIKHEF and IPHC, have provided significant effort for the testing and characterization of the pixel test structures. The experimental characterization of APTS and CE65 has proven that the process modifications combined with different pixel designs in this first run are effective to reduce charge sharing and concentrate the signal charge on a single pixel. Fig. 5 illustrates this for the APTS comparing cluster sizes for different reverse substrate biases measured in a test beam at the CERN PS. Fig 6 (a) and (b) compare the difference in charge sharing and seed signal for the CE65 test chip exposed to a ^{55}Fe radioactive source [9]:

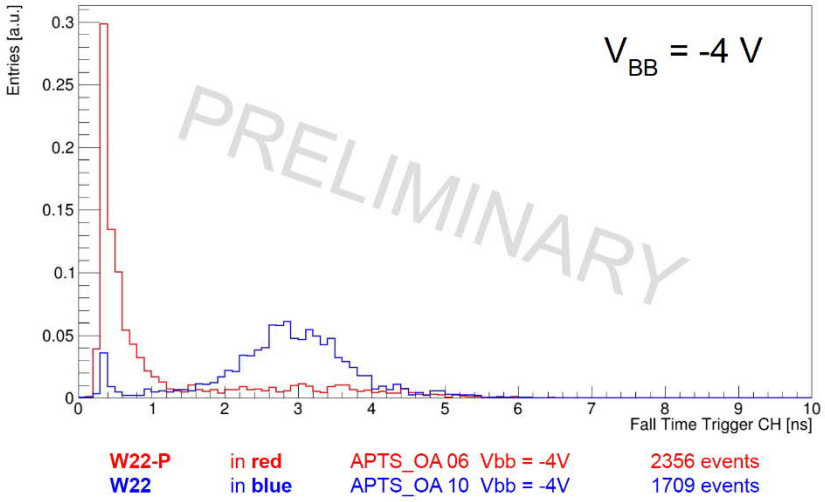
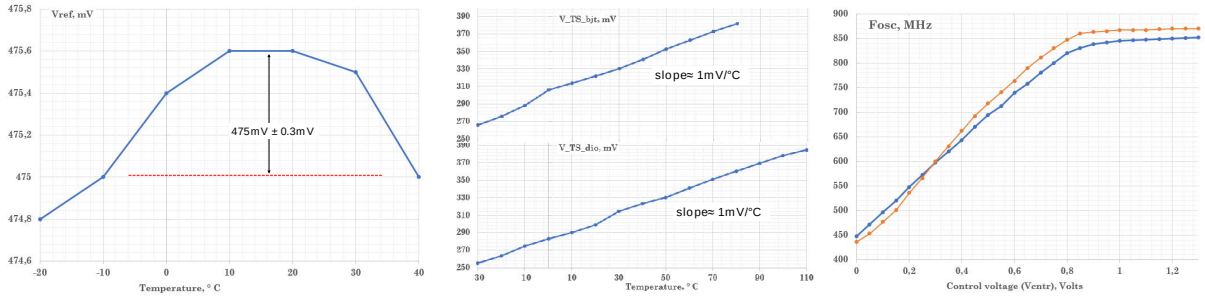


Fig 7. Comparison of single channel signal fall time after a hit on the APTS with a fast opamp readout and 10 µm pixel pitch at -4 V reverse bias, exposed to a ^{55}Fe source: blue: standard, red: gap. The addition of the low dose n-type implant with gap causes the charge of a very significant fraction of the hits to be collected well below 1 ns.

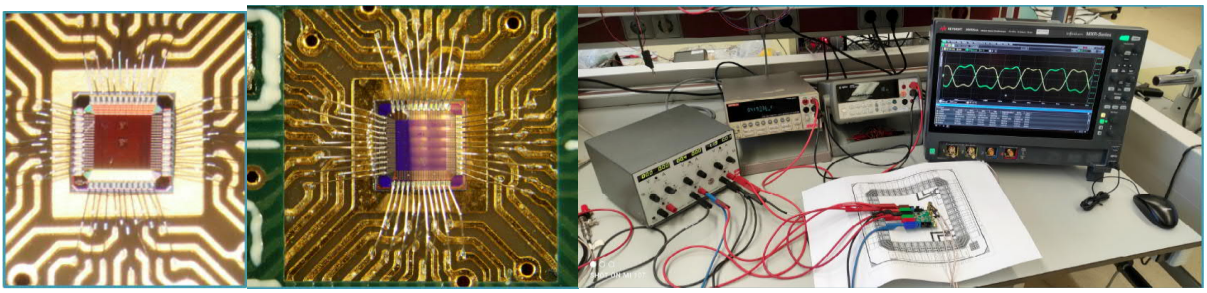
for the standard process and conventional pixel design the seed signal contains on average about 50 % of the signal, for the design with gap in the optimized process this is more than 80%. The figure illustrates also that for the latter case only the pixels sharing a full pixel edge with the seed pixel collect signal charge. Concentrating more signal charge on the seed pixel significantly improves operating margin as the charge threshold can be further increased before losing efficiency.

Fig 7 compares the signal fall times for a version of the APTS with a fast opamp readout and a 10 μm pixel pitch when the chip is exposed to a ^{55}Fe source. The operational amplifier in this version of the APTS is used to provide a high speed output stage driving a 50 ohm resistor at the pixel output. If the pixel is electrically pulsed, the signal fall time at the output is between 200 and 300 ps, indicating the speed of the circuit. The addition of the deep low dose n-type implant helps depleting the full sensitive volume, so that charge is collected by drift. The gap in the deep low dose n-type implant enhances the lateral field and further accelerates the signal charge towards the collection electrode. The acceleration of the charge collection is evident in fig. 7. For the majority of the hits the signal charge is collected well below the nanosecond for the pixel with deep low dose n-type implant, while this is not at all the case without the low dose implant. This is work in progress, the full cluster information needs to be studied to fully understand why the fall time for some cases is significantly higher, which may be related to charge collected by diffusion from the substrate. Preliminary values of conversion gains of 100 µV/e- have been reached. These values are higher than what was achieved in the TowerJazz 180 nm process, and they indicate a sensor capacitance well below 2 fF.



(a) (b) (c)

Fig. 8. Measurements of (a) a bandgap, (b) temperature sensor, (c) Voltage Controlled Oscillator

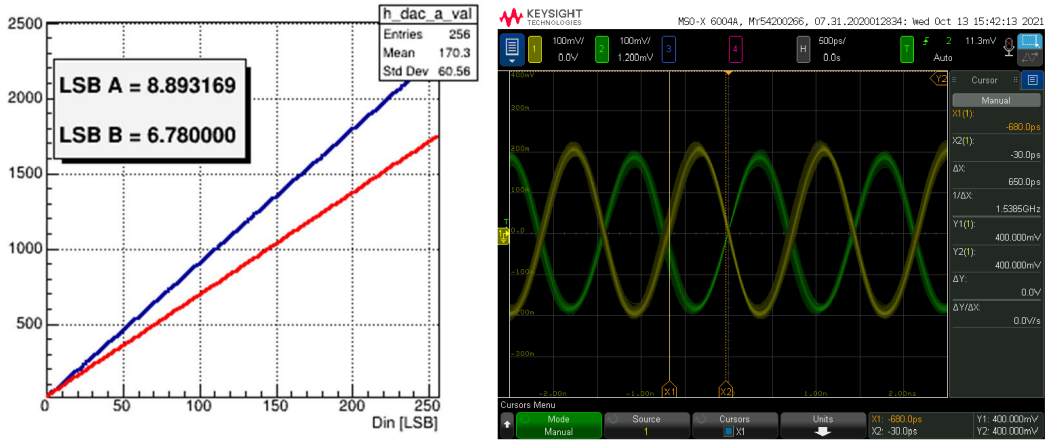


(a) (b) (c)

Fig. 9. Pictures of (a) a bandgap test chip, (b) a temperature sensor test chip and (c) the test setup for the voltage controlled oscillator.

These results demonstrate that the sensor modifications, first developed and validated on the 180nm technology, are also effective in the TPSCo 65 nm ISC technology. These enhancements are even more needed due to the thinner epitaxial layer from which the signal charge is collected.

NIKHEF designed four test chips with several flavors of analog bandgap references, temperature sensors, and a Voltage Controlled Oscillator (fig. 8,9). These blocks are useful for larger chips. IPHC designed a current DAC, STFC a CML driver and receiver (fig 10). As the figure indicates, all these circuits are fully operational. One flavor of bandgap reference and the current DAC have been adopted for use in the large stitched MOSS chip foreseen on the next submission. CPPM designed a test chip with 24 ring-oscillators to verify gate delays under different conditions. Measurements confirmed very good correspondence between different chips and post-layout simulations (fig. 11). DESY included a pixel test structure, fig. 12 shows waveforms obtained with a ^{55}Fe source indicating full circuit functionality. The pixel needs a layout correction to improve the sensor response over the full pixel area.



(a) (b)

Fig. 10. Measurements of (a) a current DACs designed by IPHC[9], and (b) a CML driver by RAL (STFC) measured at 700 MHz.

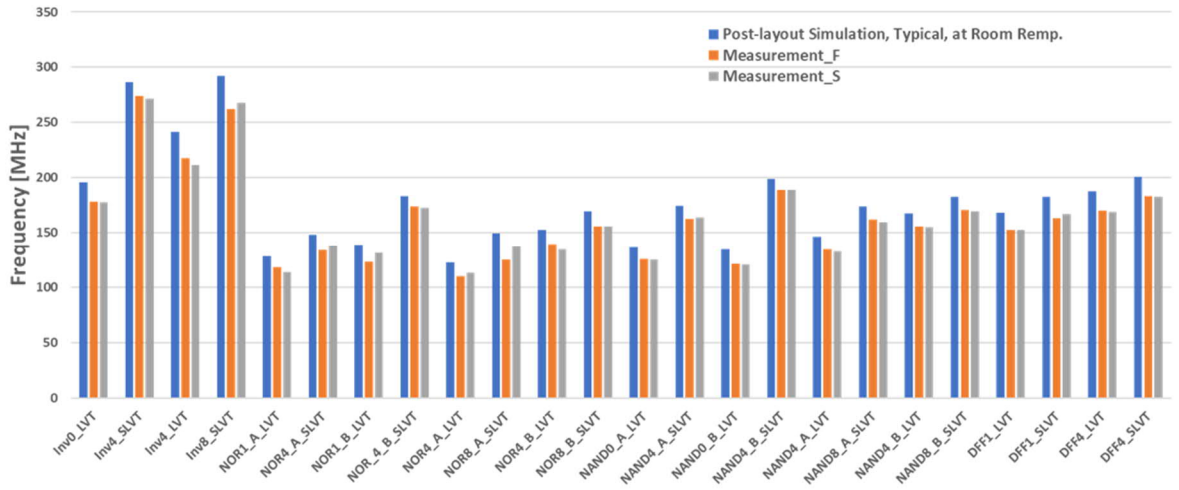


Fig. 11. Comparison between ring-oscillator measurements on two different chips and simulations.

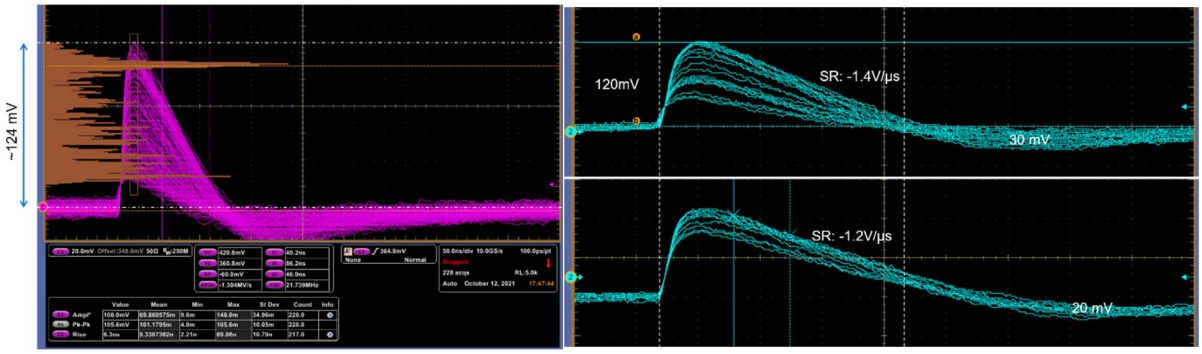
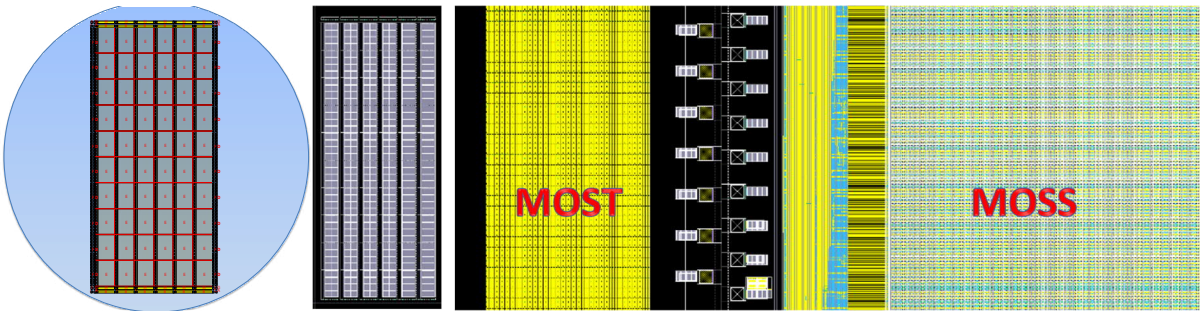


Fig. 12. Measured waveforms obtained with a ^{55}Fe source of the DESY pixel test chip (SR is Slew Rate)

2.2 Design of the first stitched engineering run ER1 in TPSCo 65 nm ISC

While pixel test structures are still being measured for more detailed sensor characterization, significant effort is put into completing the design of the next submission, engineering run ER1, with two large stitched sensors aimed at developing stitching know-how. The MOSS (MOnolithic Stitched Sensor) applies more conservative design and layout rules. It is an evolutionary design combining stitching with proven concepts to explore yield in the presence of stitching. Different pixel matrices in this 1.4 cm x 26 cm chip are powered completely independently to allow them to be turned off in case of defects. The MOST (MOnolithic Stitched Timing as it explores data and timing transmission over long distance) measures 2.5 mm x 26 cm. It contains global analog and digital power networks, where smaller sections designed at higher density (4 pixel rows in analog and one half column in the digital readout) can be disconnected from these power networks in case of defects. IPHC, NIKHEF, INFN Bari and Cagliari, Heidelberg University and CERN significantly contribute with staff to the design activities related to the stitched sensors. Several institutes make students and postdocs available, also to work at CERN with the design team. The 3 mm x 1.5 mm Hybrid to Monolithic or H2M chip designed by DESY, IFAE and CERN explores ideas deriving from hybrid pixel readout ASICs and applying them to monolithic sensors. Two dedicated test chips to study Single Event Effects have been designed by INFN Bari. This is also the case for IPHC and NIKHEF. NIKHEF will submit at least three small test chips, including an LDO, an updated temperature sensor and several versions of a 10.24 Gb/s data transmitter ported from the TIMEPIX4 design in the 65 nm TSMC technology. RAL (STFC-UKRI) will include an update of their test chip from MLR1, now further including a PLL and an I2C interface. DESY is foreseeing an update of their first test chip and another one with a small pixel test matrix. SLAC contributes with a

small pixel test chip. Several updated variants of the test chips in MLR1, the CE65 designed by IPHC, and the APTS and DPTS, will be included as well.



(a) (b) (c)

Fig. 13. Overview of the pre-mock submission of December 2021 for the next stitched engineering run with (a) an overview of the stitched chip on the full 300 mm wafer,(b) a screen shot of the layout, and (c) a zoom in to show part of the two stitched sensors MOST and MOSS.

Design for this submission is now in full swing. After significant interaction with the foundry the floorplan for this submission was finalized and approved. A pre-mock submission (fig. 13) was completed on December 22nd 2021. The feedback from the foundry has been incorporated in the design. The pre-mock submission was also very helpful practical experience with the technical flow and computing resources needed to complete DRC verification of this wafer-scale layout (in gds format).

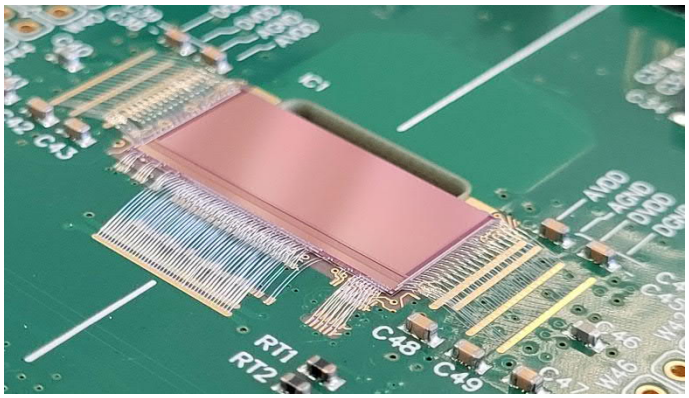
Apart from the technical aspects, significant managerial and administrative effort was necessary to prepare the ordering of such wafer-scale stitched engineering runs, including approval from CERN's finance committee.

2.3 180 nm measurements

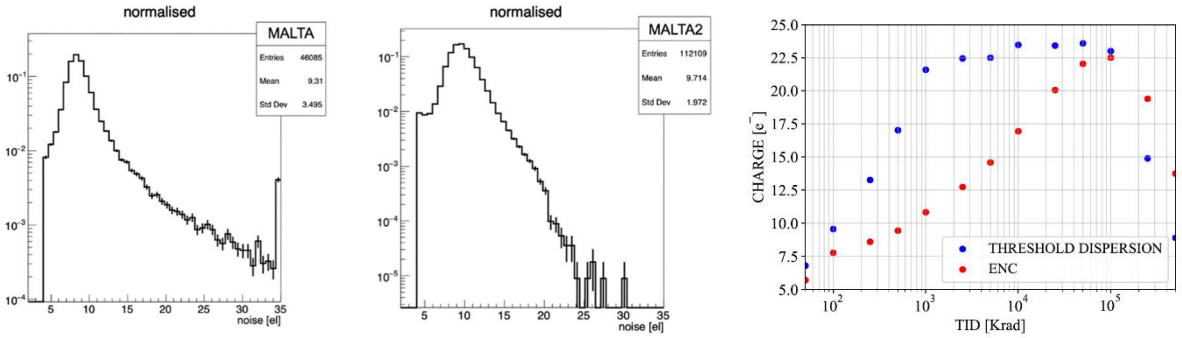
A first submission in 180 nm in 2020 included the first MIMOSIS prototype and several other chips designed in an effort led by IPHC (Strasbourg), the FASTPIX chip [5], designed by CERN in a EU-funded collaboration with INFN and Ritsumeikan University, the CLICTD chip [4] designed by CERN for the CLICdp collaboration, and a MiniMALTA designed by CERN for the STREAM project. A second submission included apart from CLICTD, FASTPIX and several MiniMALTAs, two large chips aimed at higher hit rates and significant radiation tolerance, MONOPIX2 and MALTA2, initially aimed at the Inner Tracker (ITk) upgrade of the ATLAS experiment, and designed by Bonn University, CPPM, IRFU and CERN in the framework of the STREAM project. Both engineering Runs included several process and sensor design splits, and also explored Czochralski (Cz) wafers. The front end improvement of the MiniMALTA on the first run guided the frontend modifications for the second run. Measurement results are further described below.

MiniMALTA & MALTA:

The MONOPIX and MALTA chips were developed within the STREAM project aiming at application in the outer pixel layers of the ATLAS high-luminosity upgrade. MONOPIX uses a synchronous architecture, and MALTA with a 2x2 cm^2 pixel matrix with 512 x 512 pixels of 36.4 μm x 36.4 μm, uses an asynchronous readout architecture.



(a)

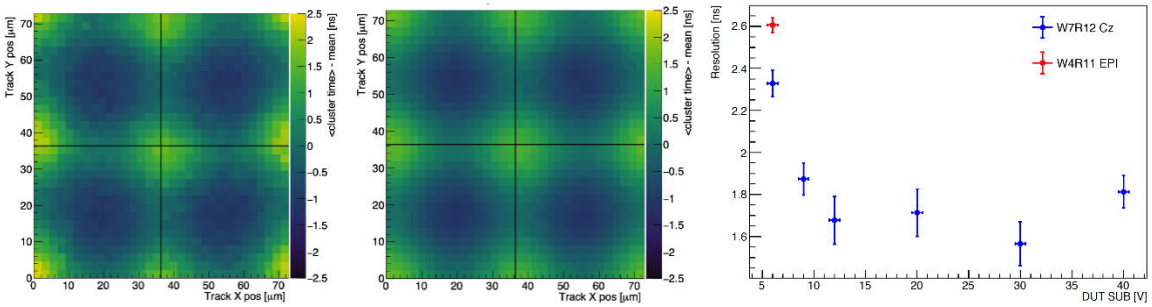


(b) (c) (d)

Fig. 14. (a) MALTA2 on board, front end noise distribution on (b) MALTA and (c) MALTA2 [10], and (d) evolution of ENC and threshold dispersion as a function of TID for a threshold around 100 e⁻ [11].

The MALTA2 (Fig. 14) front end significantly reduces the random telegraph noise tail observed on MALTA, produced in previous runs. This is demonstrated by the comparison of Fig. 14 (b) and (c) [10]. It was extensively characterized before and after irradiation, and proved to remain functional both after a $3x10^{15}$ neutron/cm^2 irradiation as well as a 100 MRad 10 keV X-ray irradiation. As an example the evolution of Equivalent Noise Charge (ENC) and Threshold Dispersion as a function of Total Ionizing Dose during the X-ray irradiation is shown in Fig. 14 (d) [11].

Significant effort was put into the evaluation of Czochralski (Cz) high resistivity bulk material, which provides a thicker sensitive layer at larger reverse substrate biases and hence a larger signal charge for MIPs (see also the CLICTD measurements). Fig. 15 (a) and (b) illustrate late arrival of signal charge for hits on the pixel edges on both epitaxial and Cz MALTA samples with low dose n-type implant with additional deep pwell implant at the pixel edges [12]. The pixel size is 36.4 µm x 36.4 µm. At higher reverse bias, only possible on the Cz sample, the time resolution improves significantly for the Cz sample as the larger signal overcomes the timewalk limitations of the front end: Fig 15 (c) illustrates this for a Cz MALTA sample with a blanket deep low dose n-type implant and a 30 µm thick epi sample with gap in the deep low dose n-type implant. Time resolution is 2.60 ± 0.05 ns on the epi sample at -6 V, and 1.7 ± 0.1 ns between -10 V and -30 V on the Czochralski sample. It has to be noted that the MALTA only provides time of arrival information without time over threshold precluding further time correction.



(a) (b) (c)

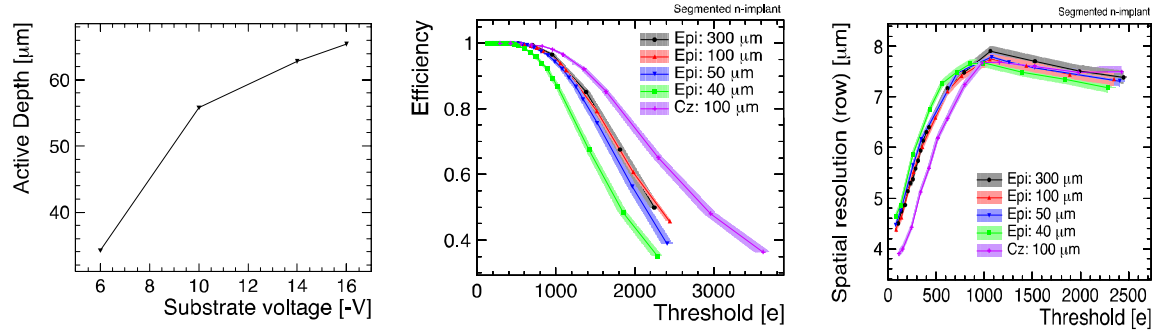
Fig. 15. Late arrival of charge from the pixel corners in MALTA for (a) Czochralski and (b) epitaxial material, both measured at a -6 V reverse substrate bias [12], and (c) time resolution as a function of reverse bias clearly showing the advantage of Cz at large reverse biases.

CLICTD

The 180 nm TJ technology demonstrator CLICTD [13] targets the requirements of large-area trackers for future Higgs factories. In 2021, the performance of CLICTD sensors with different thicknesses and substrate materials was investigated in beam tests.

Originally, the CLICTD sensor was fabricated using a 30 µm high-resistivity epitaxial layer on top of a low-resistivity substrate [14,15]. The thickness of the epitaxial layer limits the maximum depletion depth to approximately 20 µm according to simulation studies. Consequently, the active sensor depth, from which charge carriers contribute to the signal, is limited to about 30 µm, as determined from grazing angle measurements. New CLICTD samples produced using a high-resistivity Czochralski substrate offer a larger depletion depth that scales with the substrate bias voltage. As a result, the active sensor depth is more than twice as large at -16 V bias voltage compared to sensors with epitaxial layer (cf. Fig. 15 (a)) and therefore a larger signal is obtained.

To evaluate the effect of varying sensor thickness, CLICTD samples with an epitaxial layer were thinned from their nominal thickness of 300 µm (including a 10 µm metal layer on top) to 100 µm, 50 µm and 40 µm. The thin sensors minimize multiple scattering and are thus beneficial for improving the tracking performance.



(a) (b) (c)

Fig. 16. (a) Estimated active sensor depth as a function of the substrate bias voltage for a CLICTD sensor fabricated on a high-resistivity Czochralski (Cz) wafer. (b) Measured hit detection efficiency and (c) spatial resolution as a function of the charge threshold for CLICTD sensors with epitaxial layer (Epi) and different sensor thicknesses as well a high-resistivity Czochralski sensor at a substrate bias of -6V.

Due to the limited active depth, the 100 µm and 50 µm thick sensors exhibit a performance similar to the 300 µm sensors, as illustrated in Fig. 16(b) for the hit detection efficiency as a function of the

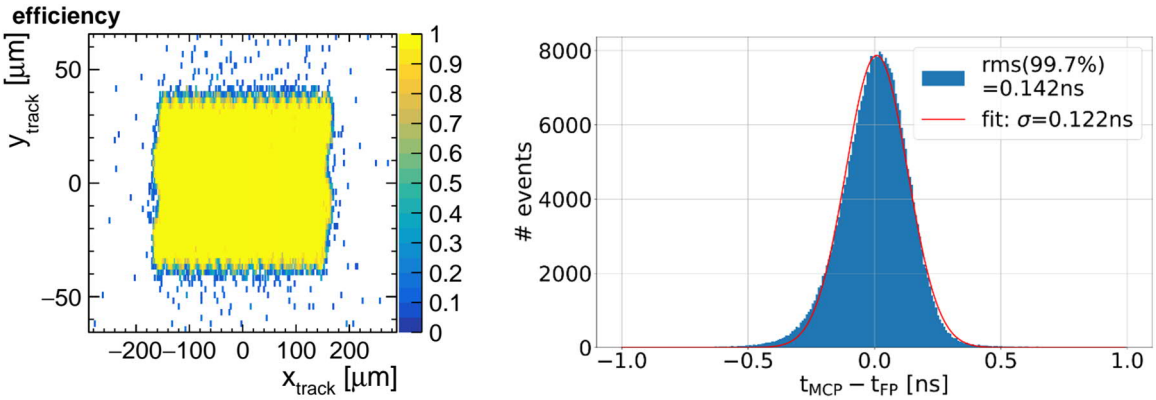
detection threshold. For the samples thinned down to 40 µm, the active sensor volume is reduced resulting in a narrower fully-efficiency operation range.

The 100 µm thick sensors fabricated on high-resistivity Czochralski substrate exhibit a considerable improvement in efficiency at high detection thresholds as a direct consequence of the larger active depth giving rise to a higher signal even at -6V substrate bias voltage (Fig. 16(b)). Also the spatial resolution profits from a higher signal provided by the high-resistivity material giving rise to a larger cluster size, and an improved position reconstruction based on charge interpolation (Fig. 16(c)).

The spatial resolution improves by approximately 15% at the minimum operation threshold. Likewise, the time resolution improves by about 10% despite limitations in the front-end electronics.

FASTPIX

After the process modifications for full depletion of the sensitive layer in 180 nm, and adaptations for CLIC and ATLAS, the FASTPIX project was started for further timing improvements. The FASTPIX prototype is equipped with 32 pixel matrices, each with 4 pixels connected to a fast analog output and 64 pixels read out digitally. Pixel pitches are 8.66, 10, 15 and 20 µm, collection electrodes are placed on a hexagonal grid. The 64 pixels with digital readout in a matrix are arranged in a 4x16 layout with 4 additional pixels connected to fast analog outputs.



(a) (b)

Fig. 17.(a) Sensor efficiency and (b) time residuals after timewalk correction for the inner region of a 20 um pitch matrix.

The FASTPIX chip was investigated in several test beam campaigns at the CERN SPS in 2021 [16]. Measurements on a 20 µm pitch matrix achieve full efficiency inside the matrix (Fig. 17 (a)) at a threshold of 74 ± 16 e and a noise of 8 ± 2 e. A time resolution of approximately 500 ps before and 120 ps after timewalk correction (Fig. 16(b)) was measured using a MCP-PMT as timing reference.

The hexagonal layout reduces the number of neighboring pixels and charge sharing, as can be seen in the cluster size (Fig. 18(a)). The cluster size is limited mostly to 3 or fewer pixels, with the largest clusters observed in the corners between pixels (Fig. 18(b)).

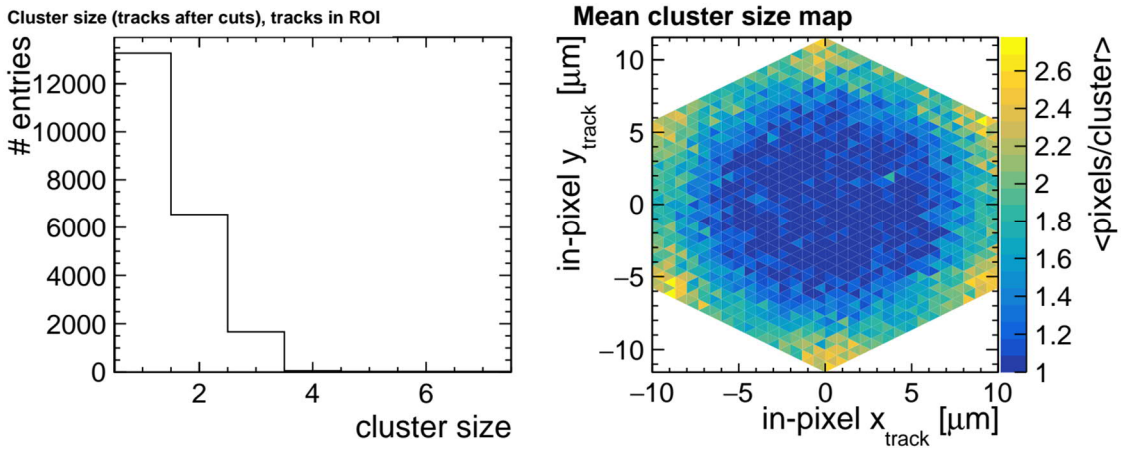


Fig. 18. Cluster size (a) distribution and (b) in-pixel map.

It was already stated that the pixel sensor modifications validated in 180nm technology are generally applicable. In FASTPIX they were applied on a small collection electrode pixel to obtain precise time information, but only the first few transistors of the full readout circuit could be fitted in the pixel at the smallest pitches and the rest of the readout had to be placed at the periphery severely limiting the matrix size. Applying the same pixel sensor modifications in the 65 nm technology, as now achieved with the first MLR submission, offers access to higher circuit density, and opens the path for a more realistic readout for precise timing in larger matrices.

3. Publications and contributions to conferences and workshops

TPSCo 65 nm

Conferences

- Kluge et al., ALICE ITS3 - a bent, wafer-scale CMOS detector, Vienna Conference on Instrumentation, Vienna February 2022
- S. Bugiel et al., Charge sensing properties of monolithic pixel sensors fabricated in a 65 nm technology, Vienna Conference on Instrumentation, Vienna February 2022
- H. Wennlöf et al., The Tangerine project: Development of high-resolution 65 nm silicon MAPS, Vienna Conference on Instrumentation, Vienna February 2022

SIMULATIONS
See WP1.4

MALTA & MiniMALTA
Journals

- C. Solans et al., Radiation hard monolithic CMOS sensors with small electrodes for HL-LHC and beyond, POS, 2021, ICHEP2020, 871, https://pos.sissa.it/390/871/pdf
- A. Sharma et al., Latest developments and characterisation results of the MALTA sensors in TowerJazz 180nm for High Luminosity LHC, POS, 2022, EPS-HEP2021, 818 https://pos.sissa.it/398/818/
- F. Piro et al., A 1 µW radiation-hard front-end in a 0.18 µm CMOS process for the MALTA2 monolithic sensor, submitted to IEEE Tran. Nucl. Science.

Conferences

- C. Solans, AIDA innova, April 2021.
- L. Flores, Latest developments and characterisation results of DMAPS in TowerJazz 180nm for High Luminosity LHC, TIPP, May 2021.
- A. Sharma, Latest developments and characterisation results of the MALTA sensors in TowerJazz 180nm for High Luminosity LHCEPS-HEP 2021, July 2021
- M. van Rijnbach, Radiation Hardness and Timing Performance in MALTA Monolithic Pixel Sensors in TowerJazz 180 nm, TWEPP, September 2021
- C. Solans, MALTA monolithic Pixel sensors in TowerJazz 180 nm technology, VERTEX, September 2021
- M. LeBlanc et al., Recent results with radiation-tolerant TowerJazz 180nm MALTA sensors, Vienna Conference on Instrumentation, Vienna February 2022
- C. Bespin et al., Development and characterization of a DMAPS chip in TowerJazz 180nm technology for high radiation environments, Vienna Conference on Instrumentation, Vienna February 2022

CLICTD

Journals

- Test-beam characterisation of the CLICTD technology demonstrator-a small collection electrode High-Resistivity CMOS pixel sensor with simultaneous time and energy measurement (https://doi.org/10.1016/j.nima.2021.165396), August 2021

Conferences

- K. Dort et al., Test-beam and simulation studies of the monolithic CMOS silicon sensor CLICTD, BTTB9, February 2021
- K. Dort et al., Test-beam studies of the monolithic CMOS silicon sensor CLICTD International Workshop on Future Linear Colliders LCWS2020 (Virtual), March 2021
- K. Dort et al., Test-beam and simulation studies for the CLICTD technology demonstrator - a monolithic CMOS pixel sensor with a small collection diode, Technology and Instrumentation in Particle Physics conference TIPP2021 (Virtual), May 2021
- K. Dort et al., Test-beam studies of the monolithic CMOS silicon sensor CLICTD, ILC Workshop on Potential Experiments ILCX2021 (Virtual), October 2021
- D. Dannheim et al., Silicon pixel-detector R&D for future lepton colliders, Vienna Conference on Instrumentation, Vienna February 2022

FASTPIX:

Journals:

- J. Braach, et al., Performance of the FASTPIX Sub-Nanosecond CMOS Pixel Sensor Demonstrator. *Instruments* 2022, *6*, 13. https://www.mdpi.com/2410-390X/6/1/13
- Conferences
- E. Buschmann et al, Performance of the FASTPIX Sub-Nanosecond CMOS Pixel Sensor Demonstrator, Workshop on Pico-second Timing Detectors for Physics, Zurich September 2021

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[2] W. Snoeys et al., NIM A 871 (2020), p. 90-96, https://doi.org/10.1016/j.nima.2017.07.046
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[10] M. van Rijnbach et al., TWEPP, September 2021, https://indico.cern.ch/event/1019078/contributions/4444328/
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[14] R. Ballabriga et al., Nucl. Instr. Meth. A 1006 (2021) 165396, https://doi.org/10.1016/j.nima.2021.165396
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WP1.3 Silicon Modules

1. Introduction

The development and construction of silicon detector modules consists of many steps, combining sensor and/or front-end chips with a flexible circuit and connection off-module as well as providing the interconnection between the different parts. Work package 1.3 focuses on the study and development of new module-building concepts for hybrid and CMOS pixel detectors. The activities can be grouped into four main areas:

- Studying enabling technologies: e.g. interconnections, post processing, packaging
- Building demonstrator modules
- Defining and developing Quality-Control (QC) tools and procedures as well as necessary infrastructure
- Testing and qualifying components as well as demonstrator modules

The activities are reported in the monthly work package meetings, which also provide a platform for discussion across the different sub-activities presented below.

WP 1.3 collaborates closely with other work packages on silicon in the EP R&D as well as with industrial suppliers (e.g. DISCO, PacTech, Optim, Conpart or Dexerials) and CERN services (PCB workshop, Bondlab, QARTlab, BE PCB service, EN-MME) to develop these new concepts and to foster new developments. Close collaboration with other institutes (e.g. Univ. of Geneva, CEA, IZM and FBK) as well as international collaborations (AIDAinnova, 100µPET) have already led to remarkable results and further strengthen these links. In 2021 WP 1.3 also further improved the commonly available equipment with a plasma cleaner and a silicon scriber.

Fellows and students:

At present there are two CERN fellows (F. Dachs, P. Svihra), two CERN doctoral students (M. van Rijnbach, J. Weick) and one technical student (J. Schmidt) working in WP 1.3.

2. Main activities and achievements in 2021

Using existing chips (ALPIDE, MALTA1, MALTA 2, Timepix or CLICpix) and sensors, the activities in WP 1.3 have made significant progress in 2021, namely:

- Construction and characterization of 2-chip and 4-chip large CMOS pixel detector modules with 100 µm thick chips and direct chip-2-chip data transfer in a cosmic telescope (Fig. 1 left).
- Successful assembly of dual chip modules using ACF (Anisotropic Conductive Film) and silicon connection pieces for electrical and mechanical connection.
- Connectivity studies and design of an ultra-light flex cable for multi-chip modules with 15 µm trace pitch for direct chip-on-flex mounting using ACF or nanowires.
- Validation of a single-die support-wafer bump-bonding process for CLICpix2 hybrid assemblies with 25 µm pixel pitch and with thin active-edge sensors demonstrating an excellent yield (Fig. 1 right).
- Optimisation of an ACF hybridisation process for Timepix3 assemblies.
- Setup of a Ni/Au plating process for single chips together with the Micro-Pattern Technology workshop and launching of a dedicated test program for both small- and large-pitch applications.
- Design of dedicated chain-structure devices for systematic plating and interconnect-yield studies.

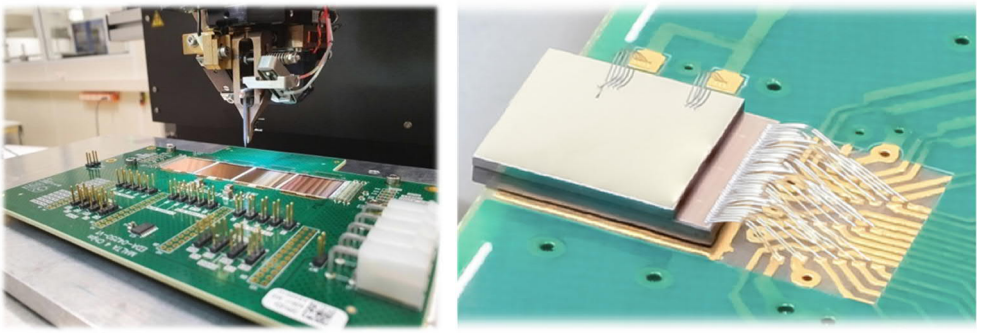

Fig. 1: 4-chip MALTA module with direct data connections between chips (left) and CLICPix2 assembly with thin active-edge sensor (right).

The following sections will report in more detail on the different R&D activities, starting with processing related tasks, followed by assembly techniques and interconnection technologies and finally module and packaging related work.

2.1. Thinning and dicing

In 2021 a total of 13 wafers (100 um and 300 um thick) have been sent for dicing, containing different monolithic pixel chips such as MALTA2, MONOPIX, FASTPIX and CLICTD.

The dicing was carried out using stealth laser dicing which allows the dicing of complex reticle layouts (Fig. 2c), contrary to saw dicing, where chips would either need to be sacrificed in the process or several dicing passes with retaping would be required. Over the course of the last two years this process has been established as standard for the samples used in the WP 1.3 activities and is now used on a regular basis.

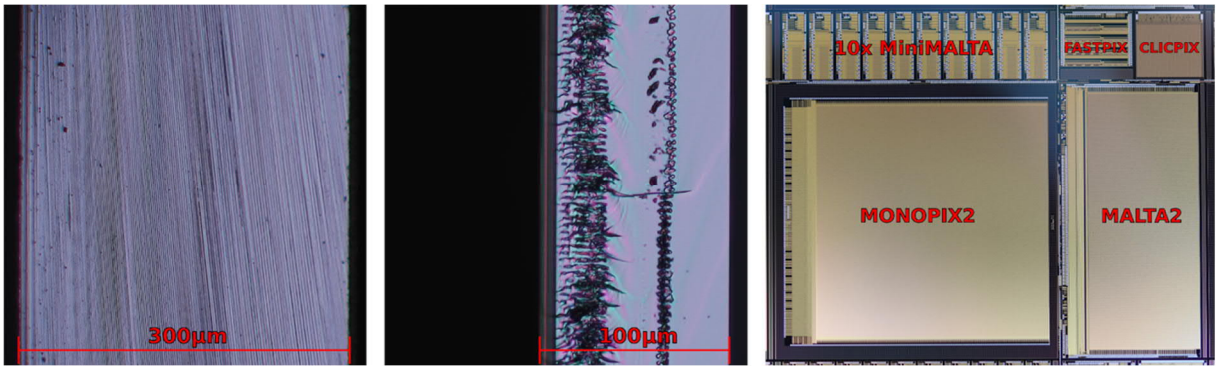

Fig. 2: Blade diced edge of a 300 µm thick chip (a) and laser diced edge of a 100 µm thick chip (b). Reticle layout of the STREAM2 run with multiple chips per reticle (c).

2.2. Plating studies

Metallisation studies have been performed to obtain the required surface topology for the in-house Anisotropic Conductive Film (ACF) interconnection method. The metallisation not only forms a surface with which the conductive micro-particles from the ACF form electrical connections, but the topology of the so-formed pads also has to create sufficiently large cavities into which the adhesive can flow after bonding on the flip-chip machine. The height and uniformity of the pads is therefore a decisive factor for a high-yield connection.

An in-house single-die Electroless Nickel Immersion Gold (ENIG) plating process is currently being adapted and optimized for various sample types (Timepix3, CLICpix2, MALTA) with different pad geometries (ranging from 10 to 100 µm diameter) and using different pad materials (Al and Ni/Au). The chemical plating studies are performed in the CERN-DT Micro-Pattern Technologies lab. The produced samples are investigated in top-views and cross-sections using optical microscopes (Figure 3).

Before the metallisation can take place, the samples have to be prepared by thoroughly cleaning them with acetone and in an ultrasonic bath with an alkaline detergent. Afterwards, the parts of the sample that are not to be treated (guard rings, bonding pads) are covered with a toluene-soluble paint. Samples with either bare aluminum pads or with previous wafer-level ENEPIG (Electroless Nickel Electroless Palladium Gold) metallisation are currently used to develop the process. Therefore, two different pre-treatments are necessary, adapted to the respective pad metal (Fig. 4).

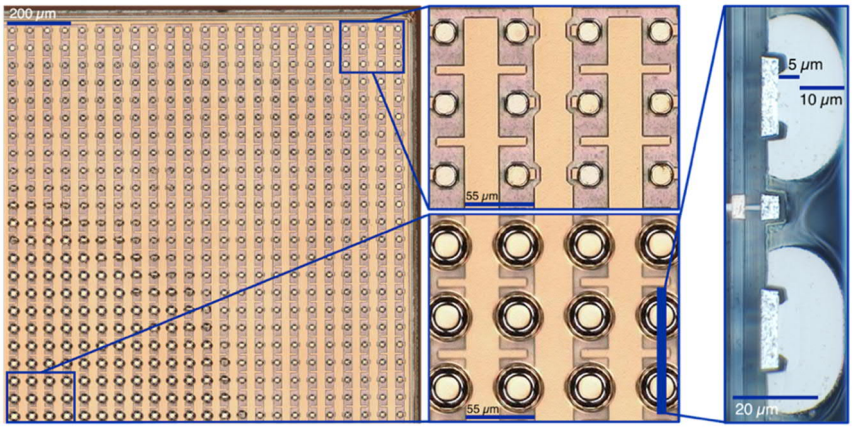

Fig. 3: Top-view of a re-worked Timepix3 chip with an uneven ENIG plating (left) and cross section of two pads with 10 µm of additional ENIG plating on top of 5 µm previous ENEPIG (right).

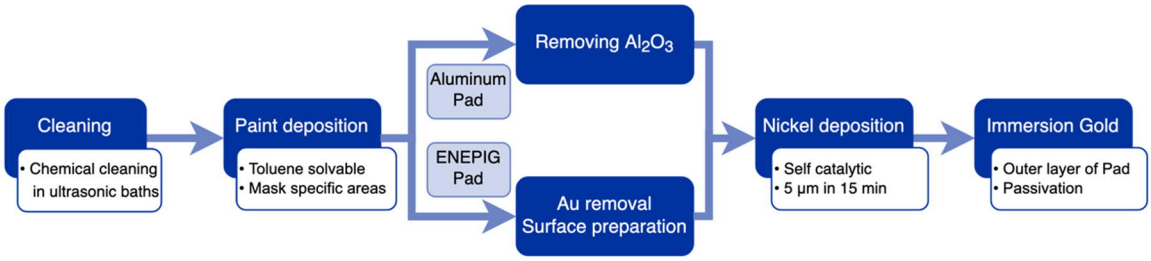

Figure 4: Flowchart of the Ni/Au plating process with a branching due to different initial pad materials.

Initial plating trials resulted in several usable samples. However, the uniformity of the pad topology (Fig. 3) and reproducibility of the process is not yet sufficient for achieving an acceptable interconnect yield in the subsequent bonding trials. The main challenges were traced back to the pre-treatment.

For the samples with bare aluminum pads, the ENIG is to be grown directly on the aluminum. For a successful plating, the passivating aluminum oxide layer must first be removed so that the surface of the aluminum pads acts as a catalyst to start the nickel growth. Ongoing studies aim at developing a reliable procedure to remove the aluminum oxide layer without damaging the thin aluminum pads, such that the widely used double zincation process can be applied. The samples with previous ENEPIG consist of gold on palladium on nickel. Current efforts focus on developing a method to re-work the previous metallisation to achieve sufficient pad heights and uniformity.

2.3. Fine-pitch hybridization

2.3.1 Solder bump technologies

The single-die support-wafer SnAg bump-bonding process for 25 µm pitch devices with 128 x 128 pixels, developed at IZM, has been further optimized and tested in 2021. This was performed using CLICpix2 ASICs and active-edge sensors of various thicknesses produced by FBK in the AIDA-2020 MPW production.

In total 8 assemblies out of 18 received have been wire-bonded to readout boards and tested in the lab: four 50 µm, two 100 µm, and two 130 µm thick sensors, with either a single floating guard ring or without guard ring.

Most of the sensors showed low leakage currents (<50 nA, one 130 µm thick sensor at ~20uA) up to breakdown voltages between -85 V and -170 V. Apart from one 50 µm thick sensor assembly with malfunctioning CLICpix2 ASIC, all devices were successfully equalized and initial tests were performed using a Sr90 source and electrical

test-pulse injection (Fig. 5 and Tab. 1). Between 0 and 27 pixels were masked per assembly because of high noise in the respective ASIC channels. The pixel response has been observed to be uniform and only one pixel without any hits from the Sr90 source but normal response to test pulses was seen in one assembly, which can be attributed to a failed bump bond. Between 6 and 14 pixels per assembly showed shorts with neighboring pixels in the test-pulse injection. This excellent overall yield of approximately 99.9% fully functioning detector channels demonstrates the high quality of the developed single-die bump-bonding process.

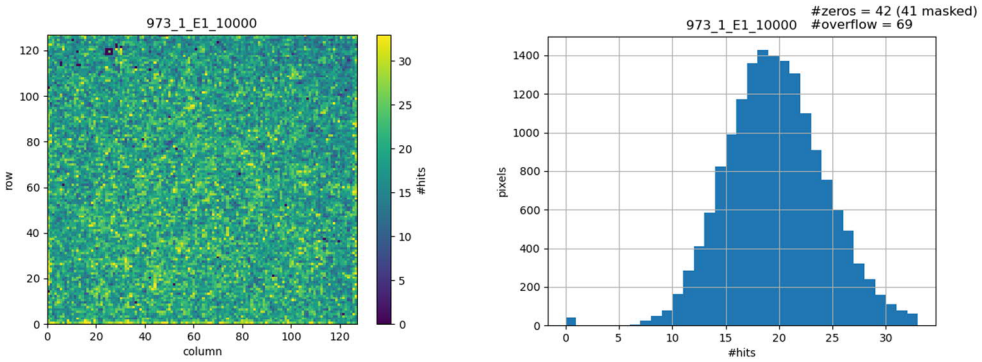

Figure 5: Results of Sr90 measurement with CLICpix2 device and 50 µm thick sensor without guard ring. The measurement consists of 10k frames with 2ms exposure time. Left: hitmap; right: pixel hit response.

Wafer	Device	Sensor Thickness	Guard ring	Breakdown voltage [V]	# of px masked	# of px w/o connection	# of px with shorts
973	1-E1 / 7-A4 3-A1 / 3-A4	50 µm	no float	-91 / -91 -160 / -161	3 / 1 0 / -	1 / 0 0 / -	9 / 11 6 / -
1185	1-E1 / 3-B3	100 µm	no / float	-88 / -170	5 / 12	0 / 0	10 / 9
3826	4-B4 / 7-A5	130 µm	no	-85 / -85	27 / 5	0 / 0	14 / 9

Tab. 1: Parameters and preliminary measurement results of the tested CLICpix2 assemblies. The number of pixels with connection issues was obtained from a Sr90 measurement with 10k frames with 2ms exposure and from test-pulse injections. Devices were biased at -60V and the thresholds set for noise-free operation. Assembly 973-3-A4 could not be operated due to a malfunctioning readout ASIC.

Beam-test measurements have been performed for some of the devices using the CLICdp Timepix3 telescope at the CERN SPS, providing a track-position resolution at the Device Under Test (DUT) of about 2 µm. A preliminary analysis of the data shows that the tested assemblies are fully functional and perform according to expectations. In the case of 50 µm sensors, the DUT track residuals at -60 V sensor bias show a box-shaped distribution with an RMS of about 7 µm (Fig. 6 bottom left). This corresponds approximately to the binary resolution of 25 µm/sqrt(12), as expected from the cluster size-distribution showing predominantly single pixel clusters (Fig. 6 top left). The overall hit-detection efficiency under these operating conditions was 99.3%, as shown in Fig. 6 right.

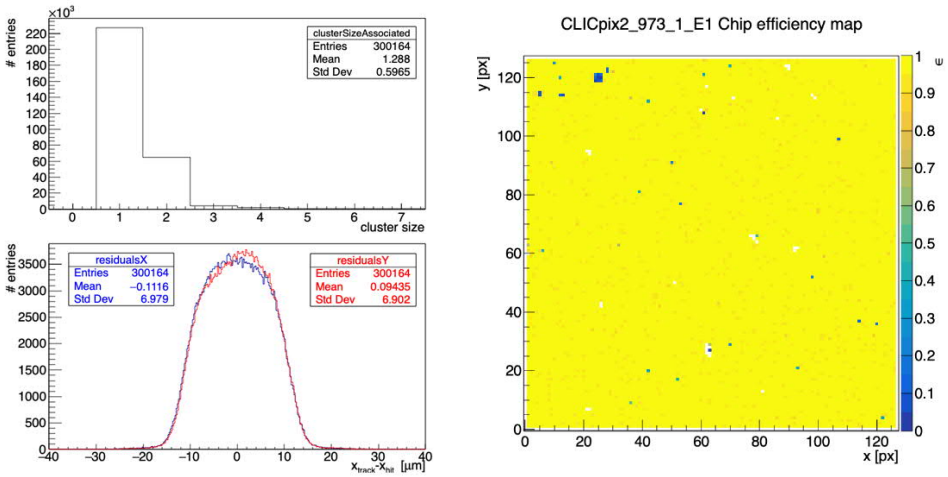

Figure 6: Top left: cluster-size distribution for CLICpix2 assembly 973-1-E1 with a 50 µm thick sensor, biased at -60 V. Bottom left: Track-cluster residuals from the same run. Right: Efficiency map of the CLICpix2 assembly 973-1-E1, biased at -60V.

2.3.2 ACF hybridization

The fine-pitch hybridization process based on Anisotropic Conductive Films (ACF) was further characterized and optimized using Timepix3 ASICs and sensors with re-worked Ni/Au plating of the pixel pads and using varying ACF film coverage areas [1].

Two of the produced assemblies were operated in the DESY test-beam facility. The observed hit-detection efficiencies across the pixel matrix confirmed the observations from earlier trials with Sr-90 source expositions. A high interconnect yield is observed for film coverages up to approximately 1 cm^2. Local degradations of the interconnect yield were traced back to the surface topology and non-uniformity of the Ni/Au plating. Ongoing studies therefore focus on the optimisation of the ENIG Ni/Au plating process (section 2.2). In addition, dedicated chain-structure devices have been designed in collaboration with FBK and the AIDAinnova project, to be used for systematic plating and interconnect-yield studies. The design of the structures with patterned metal layers on glass substrates (Fig. 7) will allow for a simplified electrical characterization of the interconnect quality using probe needles. Different sizes and pad geometries of the chain devices are implemented, mimicking the parameters of the various target applications (Tab. 2).

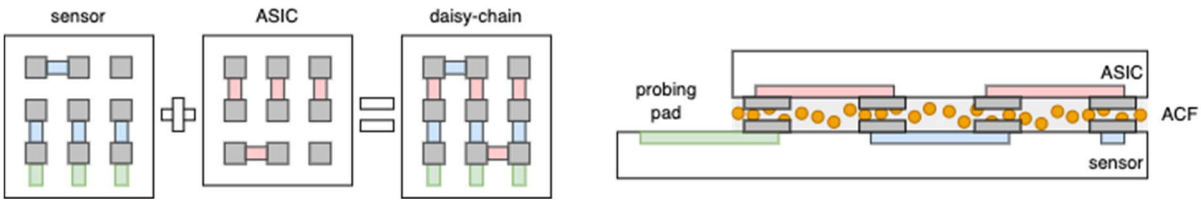

Figure 7: Schematic layout of the ACF daisy-chain structures. Left: top view; Right: cross-section.

	pitch	size in mm	connections	pairs per wafer	type	diceable
160x160 20um	20 um	3.2 x 3.2	25600	5	grid	no
CLICpix2	25 um	3.2 x 3.2	16384	6	grid	no
400x400 25um	25 um	20 x 20	640000	2	grid	yes
Timepix3	55 um	14 x 14	65536	4	grid	no

RD53	50 um	20 x 20	160000	2	grid	no
70x70 140um	140 um	20 x 20	2112	2	peripheral	yes
10x10 1000um	1000 um	20 x 20	400	2	grid	yes
3x3 4500um	4500 um	20 x 20	36	1	grid	yes

Tab. 2: List of different daisy-chain devices to be produced.

2.4. Module integration

The module integration focusses on using large area monolithic pixel chips like the chips available from the MALTA family (MALTA1 and MALTA2) with 2 cm^2 and 4 cm^2 surface area of each chip. The chips are thinned to 100 µm and diced using the process outlined in section 2.1. In a first stage the assembly of four chips in one module, covering an area up to 16 cm^2, is targeted using different techniques to transfer data directly from chip to chip over the full length.

2.4.1 Module integration with ACF

ACF has been studied as an interconnection technique to directly connect the CMOS transceiver blocks on the left and right edge of the MALTA chips to build multi-chip modules. Chips are placed next to each other at a precisely defined distance to match the pad pitch of a silicon bridge device which forms the mechanical and electrical connection between chips (Fig. 8 left).

The aluminium pads on MALTA were Ni/Au plated in a process described in section 2.2. The silicon bridge pads initially featured Cu studs with Sn/Ag tips but were later Ni/Au plated as well (Fig. 8 right), as first tests in March of 2021 showed that the Sn/Ag tips were too soft and would deform already during the ACF lamination process of the silicon bridge. Furthermore, the contact area with Sn/Ag tipped Cu studs is significantly reduced compared to fully Ni/Au plated pads.

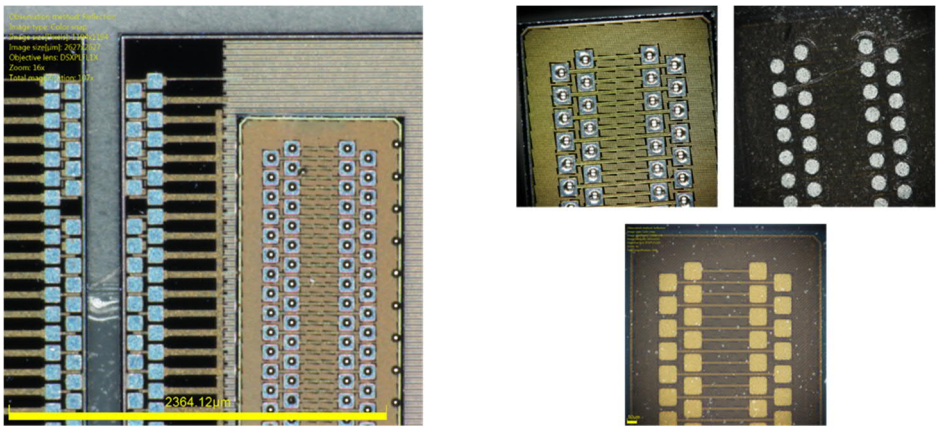

Figure 8: Two MALTA chips aligned to each other, with a silicon interconnection bridge on top of the right chip (left). Right: Silicon interconnection bridge with Cu/SnAg studs (top left), after ACF lamination (top right) and Ni/Au plated (bottom).

Based on subsequent cross section studies it was shown that a pressure of 5 kg was needed for the pads to form an electrical contact with the available ACF. Since this pressure is applied to a 1 x 5mm^2 silicon bridge, the mechanical support of the assembly during the ACF bonding process was a major challenge to overcome. Initially, chips were glued directly on a PCB prior to ACF bonding using a thermo-curing electrically conductive film, but this did not provide sufficient mechanical support. Fig. 9 (left) shows images of two MALTA1 chips with two silicon bridges connected with ACF. The top bridge has been bonded using a 5 kg setting indicating breakage of the

MALTA chips (arrows pointing at the breakage lines). The bottom silicon bridge in Fig. 9 (left) has been bonded with a 1 kg setting, not indicating any breakage lines. Detailed metallurgical cross section analysis (Fig. 9 right) showed that while the connection between the chip pads and the silicon bridge pads is well established with the 5 kg setting, the 1 kg setting was not sufficient to connect the two parts.

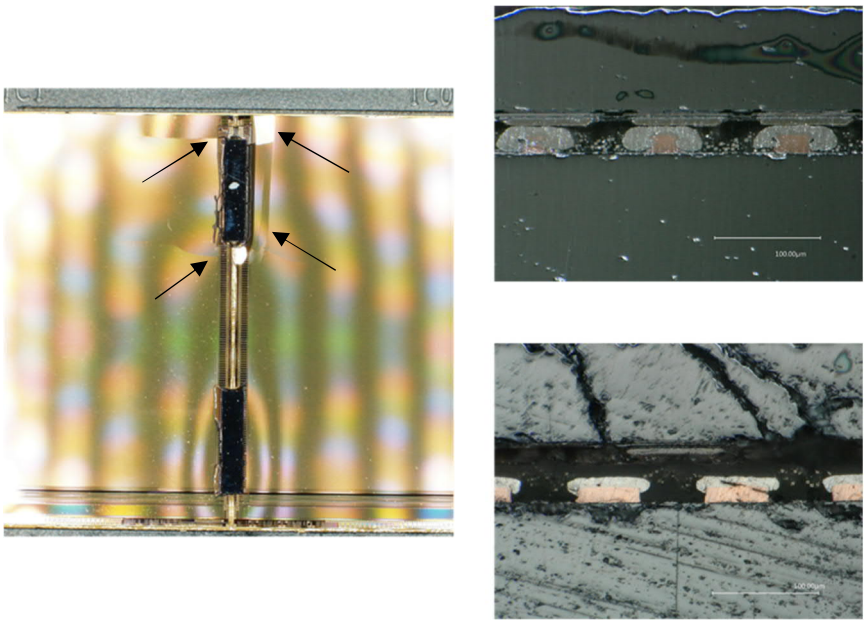

Figure 9: Two MALTA chips aligned to each other, with a silicon interconnection with 2 bridges (left) at 5 kg pressure. Crack lines in the MALTA chip are indicated by the arrows. Right: Cross section analysis of 1 kg (top) and 5 kg (bottom) pressure during the flip chip process.

The issue of mechanically damaging the chips with a 5 kg setting could be traced back to insufficient mechanical support on the flip chip machine and could be resolved by designing a dedicated SiC vacuum chuck. Up to four MALTA chips can be placed on this new chuck and held in place for the ACF bonding procedure (Fig. 10). The first assembly was produced in December 2021 on the new chuck and a 5 kg setting using dummy chips. No mechanical damage was visible in the microscope inspection. Further tests are currently ongoing, using functional MALTA chips as well as investigating alternative ACF films that will require lower pressure settings to reduce the risk of mechanical damage.

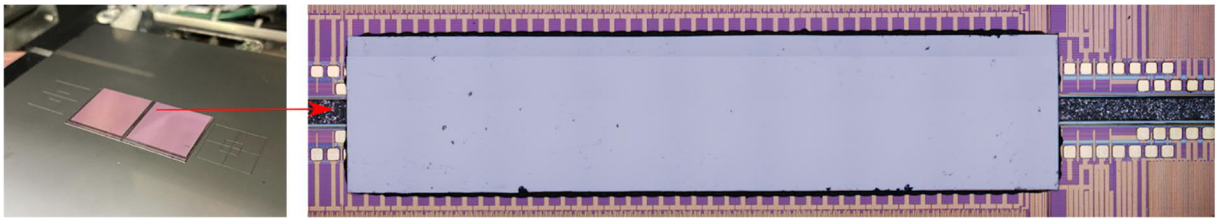

Figure 10: Two MALTA chips aligned to each other, with a silicon interconnection bridge on the SiC chuck of the flip chip machine (left). Microscope view of the silicon bridge connected to two MALTA chips using ACF.

2.4.2 Multi-chip modules with chip-2-chip connections

In preparation for the tests of multi-chip modules, the front-end parameter space has been scanned to find the optimized performance settings based on the chip condition. The procedure has been formalized and validated using single chips in different conditions, e.g. temperature and under X-ray irradiation. This will accelerate the time needed for setting up the modules for lab tests as well as in the test-beam.

Assembly and test of 4-chip modules

An important step in the development of large-area light-weight modules with pixel chips from the MALTA family is the successful assembly and characterization of a 4-chip module. The connections have been realized using ultrasonic wire bonding as a well-established technique to study the module performance. Alternative interconnection techniques (see section 2.4.1) offer better scalability for many and dense connections as well as mechanical robustness. However, the electrical characterisations of these alternative technologies are still under way.

An adapted carrier PCB with dedicated power domains allows to power chips individually by placing jumpers on the board. The design of this PCB has been adapted following the power-domain measurements which evaluated the minimum power configuration needed to check if a chip is functional. Thanks to the support of the Bondlab, the first fully functional MALTA 4 chip board was assembled in late November. Source scans across the entire module show that the data transmission between chips is working, reading out all chips via the right-most master chip only, see Fig. 12. The data are transferred using the CMOS transceiver blocks (pulse width of 1 ns) located on the left and right edges of the chips.

The arrival time of the signal varies depending on where the hit was registered on the module (Fig. 13). Within the chip the arrival time scales with increasing row number, while across the chips in a module, the arrival time scales with the distance from chip 0 that is receiving all the data from the other chips. Fig. 13 shows the time of arrival (ToA) of the signal as function of the row position for each of the chips for one of the eight sectors on the MALTA1 chip (sector 5, PMOS reset). All chips transmit the data via CMOS transceivers to chip 0 which is then read out via the LVDS contact pads.

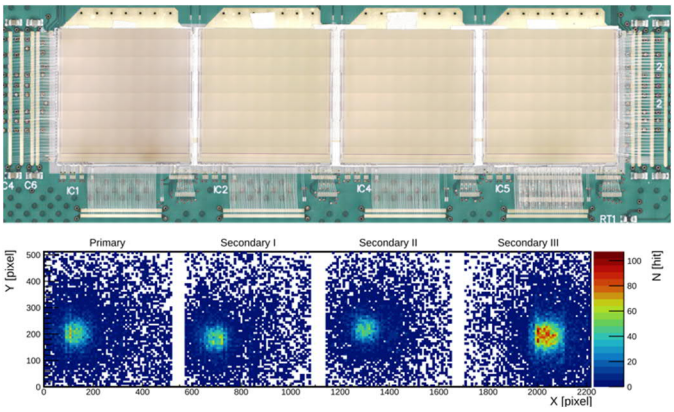

Fig. 12: New four chip MALTA module with data transfer from chip to chip to the end of module (top). Source spot (Sr90) measured on each of the chips, reading all data only via one chip at the end of the module (bottom).

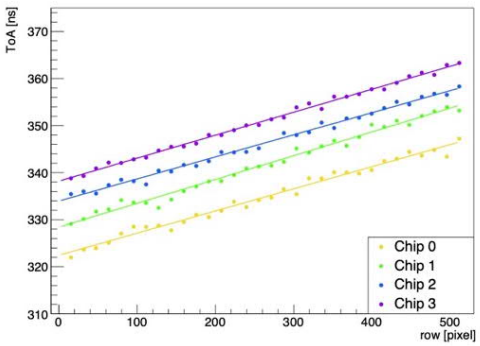

Fig. 13: Time of Arrival (ToA) of the hits registered in the different chips across the module with respect to the readout on the last chip (chip 0) for sector 5 of the MALTA 1 chip.

The MALTA multi-chip modules have been tested in a small-scale telescope in two different set-ups. The first consisted of a dual-chip module as a top plane and three single MALTA chips as tracking planes. The second set-up consisted of a quad board as a top plane, followed by two dual-chip modules, and finally a single MALTA chip as bottom plane. Figure 14 shows the event reconstruction of both set-ups where a cosmic muon track is reconstructed in all four planes. In both setups the top plane was the Device Under Test (DUT) to increase the geometrical acceptance during data taking. Data was taken with cosmic muons and at room temperature.

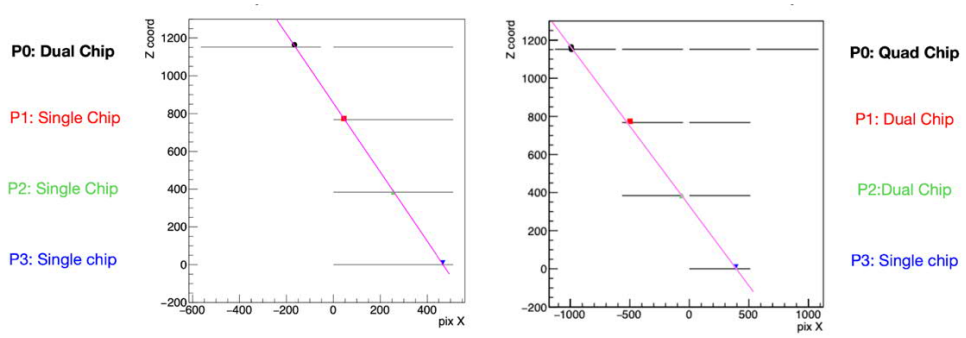

Fig. 14: Event reconstruction in a small-scale telescope with two different MALTA multi-chip module set-ups. The purple line indicates a reconstructed cosmic muon track which traverses through all four planes (P0-P3).

Fig. 15 shows a 1D efficiency map of a dual chip as a DUT in a four-plane setup with three single MALTA chips as tracking planes. This image shows that the efficiency is fully recovered before and after the gap that separates the two chips. Though the left side of the left chip suffers from low statistics due to the geometrical acceptance of the DUT with the bottom planes, a large area of the dual-chip module achieves an efficiency above 90%. Further tests in a particle test beam are planned for 2022.

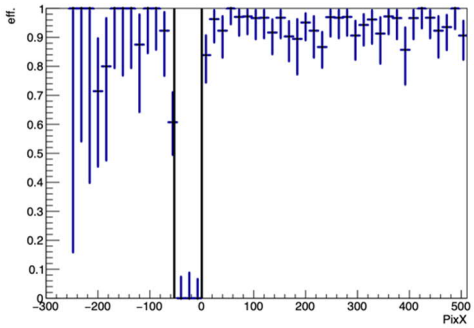

Fig. 15: 1D efficiency map of a dual chip module in x-direction. The gap size is limited by the wire-bond length that interconnects the two chips. The range extends from -300 pixels to +500 pixels due to the geometrical acceptance of the boards with the other tracking planes.

Module flex development and advanced packaging technologies

In a next step the feasibility to build a compact light-weight monolithic pixel module is addressed with a flexible PCB with four MALTA2 sensors (Fig.16). This flex will allow for mounting the sensors face-down onto the flex using pad-to-pad interconnection technologies such as ACF. The packaging will address the requirements of a minimal material-budget package, dense chip packaging of large area chips and a highly-flexible mechanical structure, while including multiple test and debug options. Further, the PCB features the chip-to-chip data transfer of MALTA2 via the CMOS transceivers at the sides of the chip.

Due to the chip pad layout and spacing this packaging approach requires a highly sophisticated manufacturing and bonding technology with a track width and clearance down to 15 µm. Several technologies including standard BGA type soldering as well as advanced ACF were assessed and a dedicated test structure has been designed to evaluate the interconnection yield.

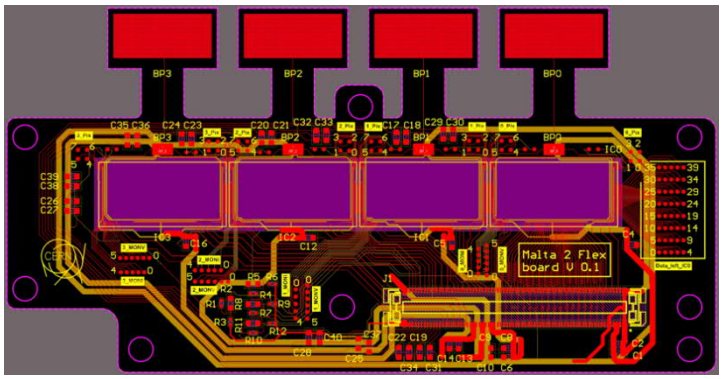

Fig. 16: Flex design for a compact module with four MALTA2 chips and using advanced interconnection technologies.

A detailed survey of interconnections provided by commercial suppliers has shown that both the chip pad size and the pad pitch limit the usable interconnection technologies for a compact module packaging and thus imply the use of advanced techniques. The application of a ReDistribution Layer (RDL) on the sensor top would allow to enlarge the pad size and pitch, opening the possibility to use more standardized interconnection technologies.

Nevertheless, the load of the interconnections on the CMOS transceivers needs to be evaluated to maintain the signal quality. A simulation (Fig. 17) has been set up to evaluate the influence of the applied load of different interconnection technologies as well as an RDL on the ASIC CMOS communication and to quantify the maximum applicable load. The results of these studies will be used to qualitatively compare the data transmission capabilities of different interconnection technologies.

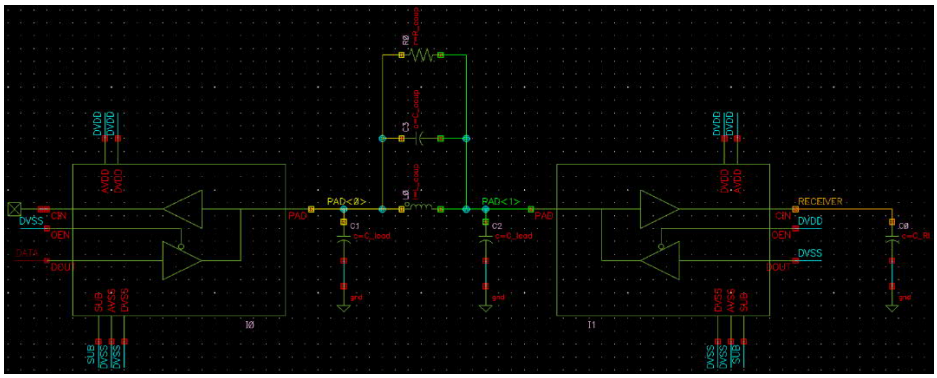

Fig. 17: Simulation model for chip-to-chip data transfer.

To further develop a compact and mechanically robust module encapsulation, studies are being carried out on two MALTA dual-chip modules using Dow Corning Sylgard 186, which is a two-component silicone [2]. While Sylgard is widely used, it is not qualified for high-radiation environments as e.g. expected in the phase II tracker regions. An alternative coating using parylene which is radiation resistant is being studied. Through Chemical Vapor Deposition (CVD) it conforms to complex shapes with a thickness that can vary between 1 µm to several mm [3]. Due to its dielectric strength, i.e. up to a few hundred MV/m, it is ideal for protecting small spaces, such as between a sensor and ASIC, as well as individual wire-bonds. In the case of hybrid pixel modules such a layer also serves to prevent sparks between the sensor and front-end.
Accelerated stress tests are planned to be performed using the climate chamber and the vibration setup available in the QARTlab, to assess the robustness of the coated test assemblies.

3. Publications and contributions to conferences, workshops, seminars

- D. Dannheim, “Silicon pixel-detector R&D for future lepton colliders”, VCI 2022, Vienna, Austria (online), https://indico.cern.ch/event/1044975/contributions/4663690/
- F. Dachs et al., “Comparative study of MALTA pixel detectors on epitaxial and Czochralski silicon”, TREDI 2021 workshop, Trento, Italy (online) https://indico.cern.ch/event/983068/contributions/4223228/

- F. Dachs, EP R&D seminar, July 2021, “Module studies with the MALTA DMAPS”, https://indico.cern.ch/event/1054861/
- M. Le Blanc, “Recent results with radiation-tolerant TowerJazz 180 nm MALTA Sensors, VCI 2022, Vienna, Austria (online), https://indico.cern.ch/event/1044975/contributions/4663664/
- P. Riedler, “Interconnection studies for monolithic silicon pixel detector modules using the MALTA CMOS pixel chip”, TREDI 2021 workshop, Italy (online), https://indico.cern.ch/event/983068/contributions/4223151/
- P. Riedler, PSD 2021 Conference, “Trends in Semiconductor Tracking Detectors” Brimingham, UK, https://indico.cern.ch/event/797047/contributions/3638214/
- P. Riedler et al., “Studies for low mass, large area monolithic silicon pixel detector modules using the MALTA CMOS pixel chip”, NIMA Vo. 990, Feb. 2021, https://doi.org/10.1016/j.nima.2020.164895
- M. van Rijnbach, TWEPP 2021 “Radiation Hardness and Timing Performance in MALTA Monolithic Pixel Sensors in TowerJazz 180 nm”, https://indico.cern.ch/event/1019078/contributions/4444328/, proceedings in preparation (JINST)
- A. Sharma et al., EPS-HEP 2021, talk, “Latest developments and characterisation results of the MATLA sensors in TowerJazz 180nm for the High Luminosity LHC”, https://pos.sissa.it/398/818/
- M. Vicente, “Pixel detector hybridization and integration with Anisotropic Conductive Films», ILCX2021, https://agenda.linearcollider.org/event/9211/contributions/49469/
- M. Vicente, “Pixel detector hybridization and integration with Anisotropic Conductive Films”, TREDI 2021 workshop, Trento, Italy (online), https://indico.cern.ch/event/983068/contributions/4223158/
- EP-DT Annual Report 2020, https://cds.cern.ch/record/2773334?ln=en, CERN-PH-DT-Note-2021-001

References

[1] M. Vicente, *Pixel detector hybridization and integration with Anisotropic Conductive Films*, ILCX2021, 2021, available at https://agenda.linearcollider.org/event/9211/contributions/49469/

[2] DOW, *Sylgard 186 Elastomer Kit,* https://www.dow.com/en-us/pdp.sylgard-186-silicone-elastomer-kit.01040286z.html

[3] SCS Specialty Coating Systems, *SCS Parylene Properties,* https://scscoatings.com/parylene-coatings/parylene-properties/

WP1.4 Silicon Detectors – Characterisation and Simulation

1. Introduction

This WP aims for enabling a fundamental understanding and optimization of the performance of particle detectors. The increasingly complex sensors and readout ASICs require improved characterization techniques, detailed modelling and simulations and a better understanding of radiation effects up to the radiation levels expected at future hadron colliders. The WP activities are performed in close collaboration with the other silicon WPs and are embedded in international R&D efforts like RD50, the LHC-upgrades, CLICdp and AIDAinnova. For the latter, the WP closely ties into several of the AIDAinnova tasks as beneficiary and/or task leader (Task 3.5. Development of common DAQ hardware, Task 4.3. Common tools for irradiation facilities quality control, Task 4.4. Design and development of a TPA-TCT characterisation system, Task 6.3. Validation of common 3D and LGAD sensor productions) as well as collaborator without beneficiary role (Task 3.3. Sub-ns timing capabilities for the EUDET-style telescopes and Task 6.3. Simulation and processing of common 3D and LGAD sensor production). The core resources provided by the EP-RD program for 2021 were one Fellow and one PhD student, which were largely extended by (part-time) Fellows and students from other funding sources at CERN and in collaboration with external institutes.

Highlights of the various WP activities in 2021 are presented in the following, covering results on silicon sensor development, characterization and simulations as well as the development of tools to achieve these tasks.

2. Main activities and achievements in 2021

2.1. The Two Photon Absorption – Transient Current Technique

The Two Photon Absorption – Transient Current Technique (TPA-TCT) is a scanning tool to study the silicon bulk with a three-dimensional resolution. The construction of the TPA-TCT setup started in 2019 and was fully commissioned in the beginning of 2021. In 2021 the setup was further extended by an infrared microscope, a cooling stage and a silicon-based energy monitor. The infrared microscope is used to picture the device under test under a highly focussing objective. The wavelength of the light used for the microscopy is 1.55 µm, wherefore the transparency of silicon is exploited to find surface layers and metallic structures even by imaging through the silicon bulk material. The cooling stage is essential for the study of irradiated DUT's, to reduce the leakage current. The silicon-based energy monitor is used as a power reference of the laser source. It is sensitive to variations in the laser's temporal profile, which was not achieved with the prior power reference.

In 2021 the TPA-TCT setup was employed in extensive studies on various silicon-based devices [1.1-1.5]. Here a Single Event Effect study campaign on RD53B chips and a charge-collection study of a strip detector are shown as examples. Further experiments conducted in 2021 are: the first TPA-TCT results of the CERN setup on irradiated PIN devices [1.3], the impact of reflection and beam clipping on TPA-TCT measurements [1.3], the study of laser aberration in different silicon thicknesses [1.4], and the study of the charge collection behaviour in LGADs with special focus on the charge carrier density related gain reduction mechanism [1.4, 1.5].

The study on the RD53B ship was a collaborative effort with the RD53 group at CERN, to investigate SEEs in digital and analogue chip regions. The TPA-TCT setup at CERN was for the first time ever used for SEE studies and the campaign was very successful. It was found that laser pulse energies up to 2 nJ do not provoke destructive effects, but SEEs were found in specific parts of the digital chip bottom. They were detected in form of phase difference shifts between the chip clock and an external clock signal due to the charge created by the TPA laser. Fig. 1.1 shows a scanned part inside the RD53B digital

chip bottom. The DUT response is colour coded, whereby yellow corresponds to SEEs and green to no-events.

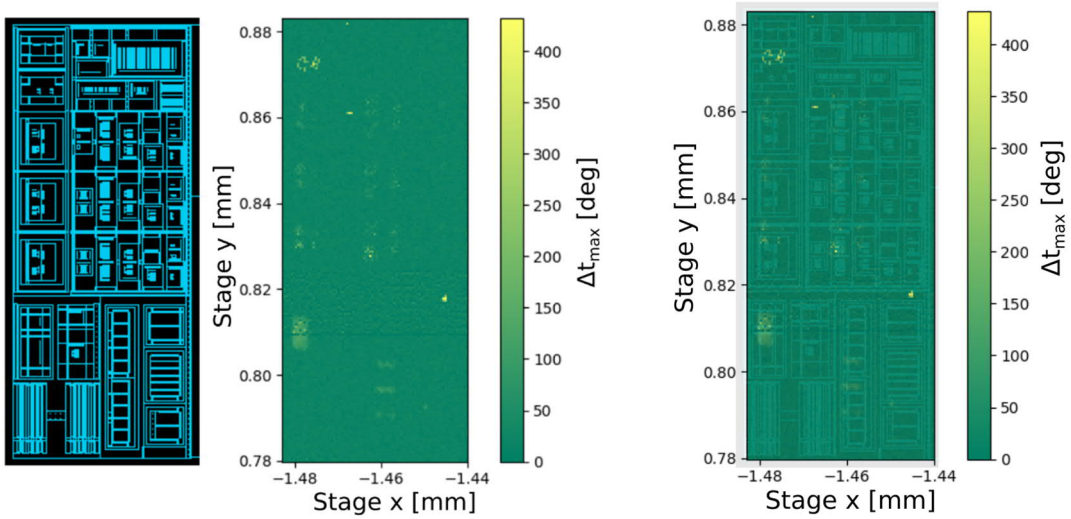

Fig. 1.1: Layout (left) and measured sensitivity map (middle) of a part of the digital chip bottom of the RD33B chip. Yellow corresponds to SEE (i.e. observation of a phase shift) and green to no-SEE. The superposition of layout and sensitivity map (right) leads to the identification of the chip areas sensitive to SEE.

The charge collection in a 300 µm thick strip detector was also studied [1.3]. Fig. 1.2 shows the charge collection after full depletion. A schematic of the DUT and lines for the orientation are included. The laser was injected from the backside of the DUT, therefore charge collected above the top side is related to reflection of the laser at the top side surface. The highest charge collection occurs below the readout electrode, due to laser reflection at the top-side strip metallisation. Furthermore, the impact of the weighting field from the readout electrode on the charge collection is visible. This is the first time that the charge collection in a strip detector was studied with a three-dimensional resolution by the TPA-TCT method.

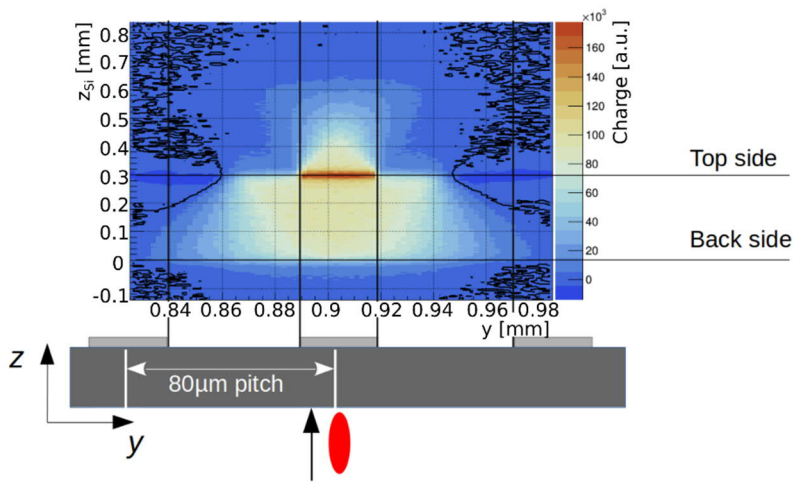

Fig. 1.2: Collected charge in a 300 µm thick strip detector. A schematic and various orientation lines are included to ease the understanding.

2.2. The Caribou DAQ system

Caribou [2.1, 2.2, 2.3] is a flexible open-source DAQ system designed for laboratory and high-rate beam tests and easy integration of new detector prototypes developed within the EP-R&D silicon work packages and the RD50 CMOS sensor studies. Several test-beam campaigns using Caribou have been performed at DESY and the CERN SPS for CLICpix2 [2.4], CLICTD [2.5], and FASTPIX [2.6] detector

assemblies. A new and more compact version of the FASTPIX chip board, better suited for test beams, was designed and used in the subsequent laboratory and test beam measurements (Fig. 2.1, left). The software was extended to perform more tasks directly on the Caribou system, for example the threshold equalization for CLICpix2. The Caribou integration of the DPTS and APTS monolithic test chips produced in the 65 nm MLR1 submission in WP 1.2 is in progress. Chip boards for the DPTS chip have been designed and produced (Fig. 1, center) and the software and firmware was adapted. First laboratory measurements with the DPTS using a high-bandwidth oscilloscope integrated into Caribou for readout were performed and test-beam measurements are foreseen in summer 2022. For the APTS chip, an amplifier test circuit was produced and tested, and the chip boards were designed and are now in production (Fig. 2.1, right). A Time-to-Digital-Converter (TDC) implemented on the Caribou FPGA is under development. This will allow for precision timing over large time spans and is required for the ToA, ToT, and position encoding used in EP-R&D WP 1.2 test chips with asynchronous readout, which is currently limited by the oscilloscope readout.

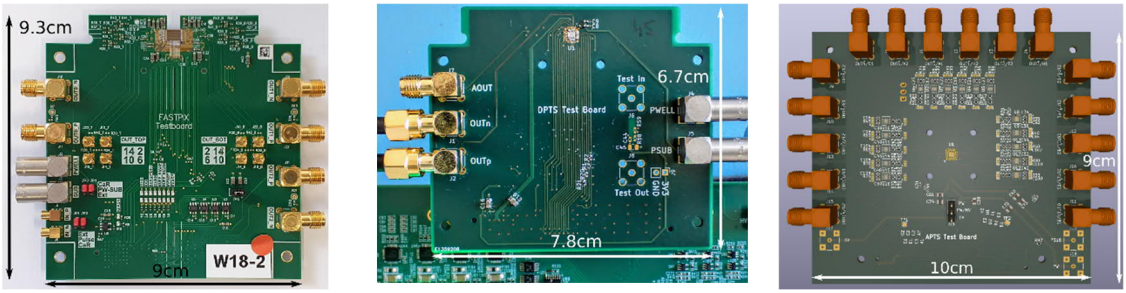

Fig. 2.1. Caribou chip boards for the FASTPIX (left), DPTS (center), and APTS (right) test chips

2.3. Study of the NIEL (Non-Ionizing Energy Loss) and displacement damage effects

This task is dedicated to the development of radiation monitoring devices and the study of the Non Ionizing Energy Loss (NIEL) concept. NIEL functions for Silicon, previously established in RD48 [3.1.], are used to compare and scale the damage impacted on devices in different radiation fields and is used for the prediction of detector damage by the LHC experiments. The goal is to revise the NIEL concept for better damage predictions serving both the development of radiation monitoring devices and the predictions of damage occurring in HEP experiments. A particular weakness of the present NIEL concept is that it does not distinguish the different formation rates of cluster and point defects in the silicon crystal for different particles and particle energies.

Geant4 and FLUKA simulations have been carried out in 2021 to characterize the displacement damage in silicon, for which a 100 μm thick silicon slab was placed in pencil beams of protons and neutrons of different energies. In Geant4, QGSP_BERT_HP and QGSP_BERT_HP__SS physics lists were chosen, while QGSP_BIC_HP and QGSP_INCLXX_HP were investigated as well. Primary knocked on atoms energy spectra have been analyzed in terms of Coulomb elastic, nuclear elastic and nuclear inelastic cross sections and the Lindhard's [3.2] and Xapsos-Burke [3.3] formalisms were applied to calculate the NIEL values. Fig. 3.1 shows the primary knocked-on silicon atom spectra originating from different types of scattering as obtained with Geant4 for 200 MeV protons. By integrating the spectra and summing up all the contributions, a NIEL value is obtained. A comparison of the obtained NIEL values for protons and neutrons of various energies against previous data from literature is shown in Fig. 3.1(right). Furthermore, in Geant4 custom physics described in [3.4] was used to further track the distribution of subsequent Silicon recoils. The efforts to define and quantify cluster and point defects are ongoing. Primary knocked-on silicon atoms of various energies are being investigated and a revision of the RD48 dataset, shown in Fig.3.1(right) in terms of cluster defects and point defects, is envisioned. Furthermore, electrons and gammas are planned to be investigated as well as more

detailed comparisons between Geant4 and FLUKA. Existing experimental data is reviewed aiming to benchmark the simulations.

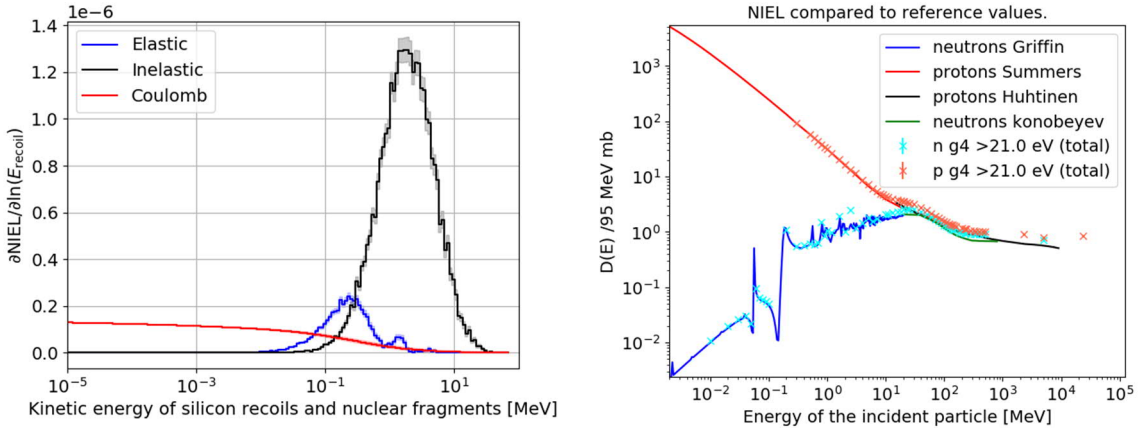

Fig. 3.1 (left) Geant4 simulation of NIEL for primary knocked-on atoms originating from coulomb elastic (red), nuclear elastic (blue), nuclear inelastic (black) scattering from 200 MeV protons as a function of recoil energy. Integrating the area under the curves yields the total NIEL. (right) NIEL values obtained for protons and neutrons of various energies.

2.4. RAdiation DAmage in CCDs for Dark Matter Searches (RADAC)

In collaboration with external experts on dark matter searches with silicon detectors, a new line of investigation has been stablished within the work package [4.1]. The final goal is to study the discrimination between nuclear and electron recoils by optically-assisted charge readout of lattice defects following ionization events, i.e. by scanning the silicon bulk of Charge Coupled Devices (CCDs) commonly used to detect dark matter interactions with ordinary matter. The main limitation for dark matter searches in such devices is the leakage current due to defects in the silicon bulk. To meet the requirements for the next generation of dark-matter silicon-based detectors, it is crucial to understand the origin of the leakage current and reduce it by at least one order of magnitude. A set of CCDs have been already selected, characterized and packaged. In the next few months, we will start a campaign to properly characterize the population of defects present in the devices using the Transient Current Technique (TSC), and if possible also employ other techniques such as DLTS and TPA-TCT.

2.5. Defect spectroscopy studies on LGADs

Low Gain Avalanche Diodes (LGADs) operating in a high radiation environment undergo a degradation in performance that is linked to defects formed during the particle-device interaction. Those defects (like the boron-interstitial-oxygen-interstitial defect BiOi) result in a deactivation of active boron in the gain-layer region. However, the boron deactivation in LGADs cannot fully be understood using the common defect kinetic model that assumes BiOi being the main responsible defect inducing acceptor deactivation [5.1]. In this context the question of additional boron-related defects formed in the highly boron-doped gain layer region of a LGAD came up. To obtain information on those boron-related defects, the applicability of defect-spectroscopy methods on LGADs was examined. In this context Deep-level-transient spectroscopy (DLTS) and Thermally Stimulated Current (TSC) measurements were performed at CERN on irradiated and non-irradiated LGADs from different foundries (FBK, CNM, HPK).

DLTS is a technique that measures capacitance transients (measurement frequency 1 MHz) at low temperatures (down to 20 K). The capacitance measurements, shown in Fig. 5.1, reveal that due to a strong frequency and temperature dependence of the gain-layer capacitance data obtained by DLTS are very difficult to analyse. However, TSC could successfully be used to identify radiation induced defects in LGAD devices as it is based on current measurements originating from thermally stimulated

charge carrier emission from defects and therefore is not depending on the capacitance of the device. But also with this technique the discrimination between gain-layer and high-resistivity Si-bulk defect contributions remains very challenging. Fig. 5.2 shows TSC spectra of two LGADs, irradiated at different fluences. Radiation induced defects in the temperature range of 20K to 120K can be seen clearly. However, it must be noted that due to the gain layer of the LGADs the detected current signals are amplified. That becomes obvious e.g. in the increase of the background leakage current, that starts for the lower irradiated LGADs, for which the gain layer is not strongly damaged, already at temperatures > 100K. This amplification effect, that shows a dependence on the applied reverse bias, hinders the exact determination of defect concentrations, which are usually used to derive defect introduction rates. Another effect that impacts on the measurements is that the defects can induce internal polarization fields in the device and influence the TSC signal leading even to a sign inversion of the current. Therefore, in a next step highly B-doped pad-diodes that mimic the gain layer of an LGAD will be produced and investigated. Those investigations together with simulations of TSC spectra could deliver further profound insight into the defect formation in LGADs.

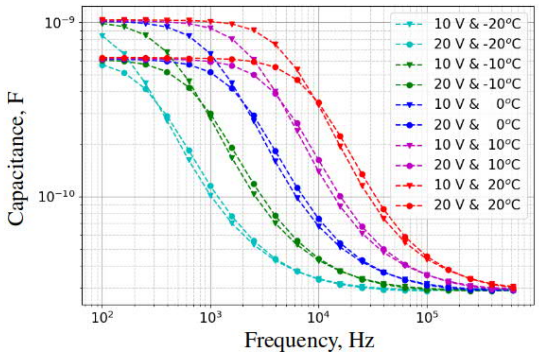

Fig. 5.1 Gain-layer capacitance values of a neutron-irradiated LGAD (fluence: 1E+14 neq/cm2) as a function of the measurement frequency and for different temperatures. With decreasing temperature and increasing frequency the capacitance drops.

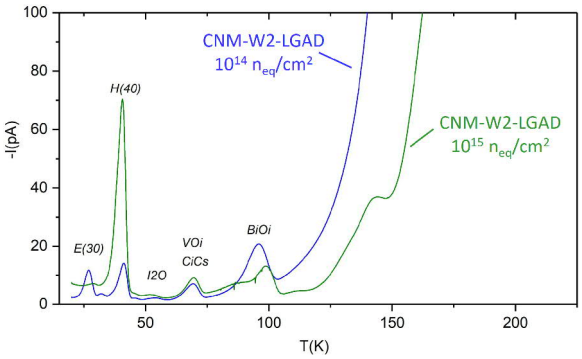

Fig. 5.2 TSC (Thermally Stimulated Current) spectra of two LGADs neutron irradiated with 1E+14 neq/cm2 (blue) and 1E+15 neq/cm2 (green). The observed defect levels are labelled by their tentative identification.

2.6. Performance and operation of LGADs before and after irradiation

Low Gain Avalanche Detectors (LGADs) are one of the most promising sensing technologies for future 4D-tracking applications. The technology has been chosen for the ATLAS and CMS HL-LHC timing detectors [6.1]. In this context, studies on radiation damage of LGADs have been performed in collaboration with the CMS timing detector group. The aim is to have a better understanding of the performance in terms of timing and collected charge after irradiation. Almost 200 LGADs and PINs were characterized at the CERN SSD lab before and after neutron irradiation up to a fluences of 2.5e15 n_{eq}/cm^2. Different producers were included in the study: FBK, CNM, and FBK, and results were presented within the collaboration and at workshops. In Fig. 6.1 the degradation of the gain layer after irradiation is demonstrated by capacitance measurements (CV) performed on sensors from HPK and CNM. It can be seen by the shift of the peak in the CV curve how the depletion voltage of the gain layer (V_{GL}) is reducing with increasing irradiation. Furthermore, a second irradiation campaign with 23 GeV protons has been performed. The results are expected for 2022 and will be compared with the previous results obtained after neutron irradiation and will allow for a more detailed study of the single event burnout effect of LGADs [6.2].

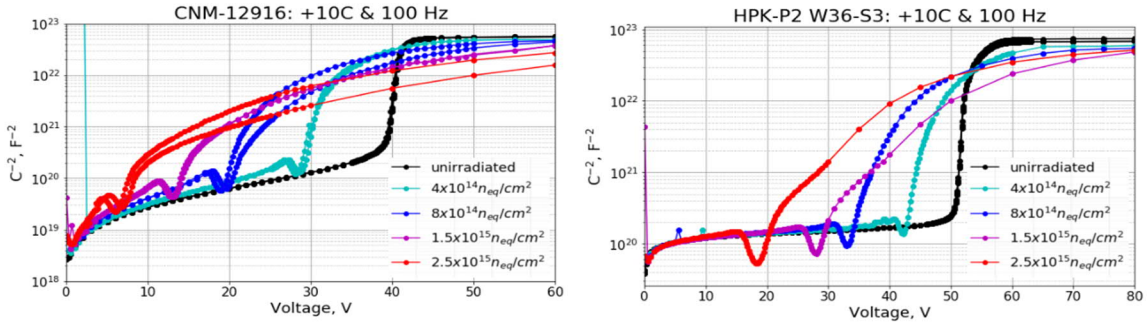

Fig. 6.1: Capacitance as a function of the voltage for LGADs from two different producers (CNM left and HPK right) before and after neutron irradiation.

Another important result was the confirmation of the gain suppression mechanism previously observed in LGADs. The studies of this mechanism were extended to more devices for a better understanding of the process. The results confirm that the gain of LGADs depends on the charge density of carriers arriving at the gain layer. With the obtained data, the phenomenon is now better understood and extensively parameterized. Furthermore, it was proven that the effect is still present after irradiation. This effect can be beneficial for the experiments if they can reduce the charge density induced by Minimum Ionizing Particles (MIPs) during their operation. This can be seen in Fig. 6.2, where the charge density arriving at the gain layer was reduced by tilting the devices. We see that in this case for a 14º angle it is possible to improve the charge collected and correspondingly the time resolution by almost 18%. These measurements were performed in the SSD lab with a Sr-90 source [6.3].

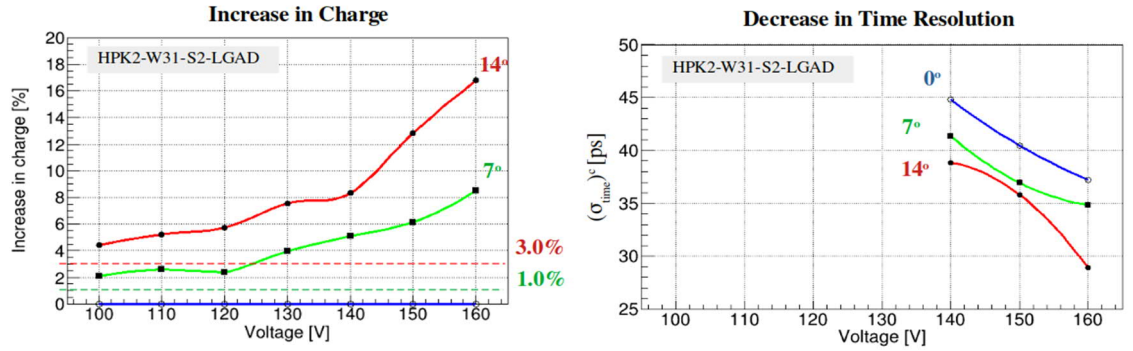

Fig. 6.2 (left): Increase in the most probable value of the measured charge, with respect to the 0o position, as a function of the bias voltage for different rotation angles. (right) Time resolution measured for the three angle configurations as a function of the reverse bias.

2.7. Advanced simulation packages

Advanced simulation tools are required to simulate, model and optimise the complex sensor designs evaluated in this work package. A combination of finite-element and transient Monte Carlo simulations is employed to enable a precise sensor modelling and high statistics of the simulation samples [7.1]. For this purpose, this work package contributes strongly to the development and maintenance of the Monte Carlo frameworks Allpix Squared [7.2] and Garfield++ [7.3].

In the past year, several new features and improvements were implemented in Allpix Squared, such as refined multi-threading capabilities or advanced models for the parameterization of charge carrier mobility and recombination [7.4,7.5]. An Allpix Squared User Workshop took place in 2021 [7.6], bringing together the Allpix Squared community to discuss new features and share results. The transient simulation capabilities of the Allpix Squared framework were investigated extensively in the past year by benchmarking them against stand-alone transient

3D TCAD simulations and test-beam data [7.7, 7.8]. The comparison of transient current pulses is illustrated in Fig. 7.1 for CLICTD sensors using three different pixel flavors. A charge injection in the pixel corners is simulated, which takes approximately 8 hours using transient 3D TCAD simulations and 0.1 – 0.2 s for the transient Monte Carlo simulations on the same machine using the same number of threads. Despite the different charge collection times and field configurations in the different pixel flavors, the two simulation approaches yield compatible results in all cases without the need for prior tuning.

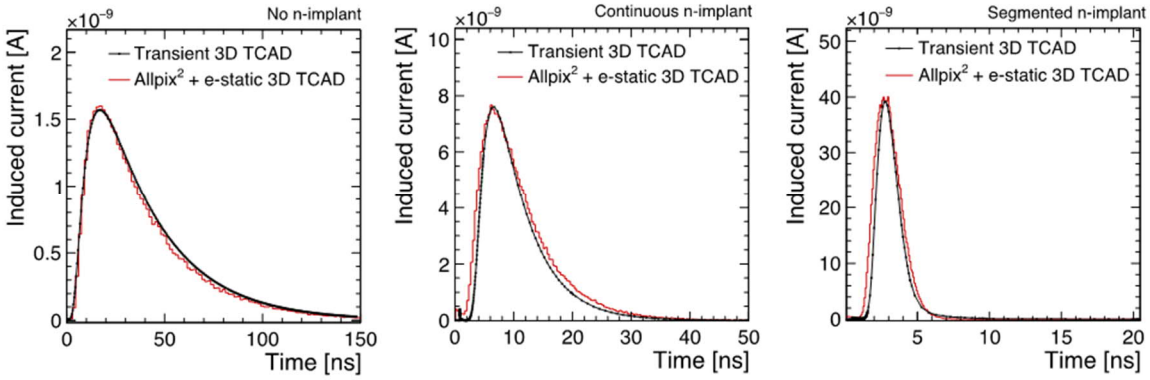

Fig. 7.1. Transient current pulses for transient 3D TCAD and transient Allpix Squared simulations after charge injection in the pixel corner for three different sensor designs (left: no n-implant, middle: continuous n-implant, right: segmented n-implant).

The small computation times for the MC simulations also enable the consideration of statistical fluctuations and secondary particles as depicted in Fig. 7.2, where the transient-pulse distribution is displayed. The pulse-by-pulse variations underline the importance of including statistical fluctuations in the simulation setup to guarantee a realistic modelling of the sensor response. A comparison between test-beam data and transient Allpix Squared simulations is shown in Fig. 7.3 for the mean cluster size as a function of the detection threshold. The shaded band reflects the systematic uncertainties related to uncertainties in the doping profiles. The agreement between data and simulation is well within the uncertainties over the full threshold range, which confirms the validity of the simulation approach. The simulations are used for further development of silicon sensors, e.g. for the optimization of monolithic 65 nm CMOS silicon sensors in WP 1.2.

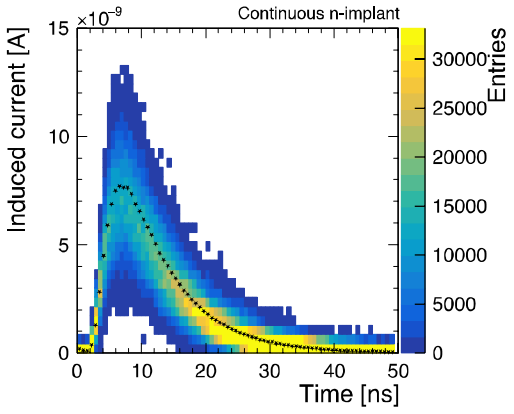

Fig. 7.2. Transient current pulse distribution using transient Allpix Squared simulations. The simulation included secondary particles and energy deposition fluctuations. The black stars denote the average pulse height.

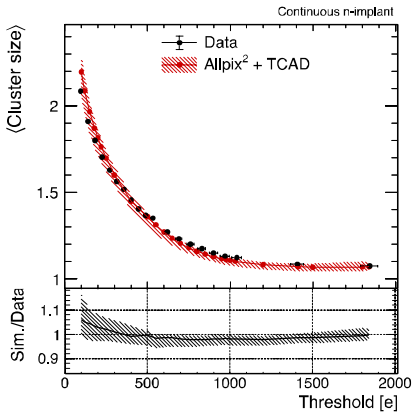

Fig. 7.3 Mean cluster size as a function of the detection threshold for data and transient Allpix Squared simulations.

3. Publications and contributions to conferences and workshops

[1.1]S. Pape et al., A table-top Two Photon Absorption – TCT system: measurements of irradiated and non-irradiated silicon sensors, 12th International Conference in Position Sensitive Detectors, Birmingham, 2021.

[1.2] S. Pape et al., Characterisation of irradiated and non-irradiated silicon sensors with a table-top Two Photon Absorption TCT system, PSD12 Proceedings, submitted in 2021.

[1.3] S. Pape et al., A table-top Two Photon Absorption – TCT system: experimental results, 38th RD50 workshop, CERN (2021), available at https://indico.cern.ch/event/1029124/contributions/4411336/

[1.4] S. Pape et al., Gain suppression mechanism in LGADs and SEE studies in a RD53B chip measured with the TPA-TCT method, 39th RD50 Workshop, Valencia (2021), available at https://indico.cern.ch/event/1074989/contributions/4601951/

[1.5] S. Pape et al., Characterisation of the charge collection in LGAD sensors with a newly developed table-top TPA-TCT system, Vienna Conference on Instrumentation (2022), Vienna - virtual, available at https://indico.cern.ch/event/1044975/contributions/4663778/

[2.2] E. Buschmann, Recent Improvements of the Caribou DAQ System, BTTB9 (2021), virtual, available at https://indico.cern.ch/event/945675/contributions/4160095/

[2.3] E. Buschmann, The Caribou DAQ System – Current Status and Ongoing Developments, TWEPP 2021 (2021), virtual, available at https://indico.cern.ch/event/1019078/contributions/4444429/

[2.5] R. Ballabriga et al., Test-beam characterization of the CLICTD technology demonstrator - a small collection electrode High-Resistivity CMOS pixel sensor with simultaneous time and energy measurement, CLICdp-Pub-2021-001 (2021), arXiv: https://arxiv.org/abs/2102.04025/

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[3.5] V. Maulerova et al.,39th RD50 workshop, Valencia, 17-19 Nov 2021, presentation, https://indico.cern.ch/event/1074989/

[3.6] V. Maulerova-Subert et al., University of Hamburg, Invited talk, Hamburg 21 Jan 2022, UHH Detector Lab.

[3.7] V. Maulerova-Subert et al., RADAC meeting, invited talk 26 Jan 2022, https://indico.cern.ch/event/1118322/

[3.8] V. Maulerova-Subert et al., Queen Mary University of London, Invited talk 2 March, 2022

[4.1] S. Juhyung Lee, RADAC - Radiation Damage to CCDs for Dark Matter searches, WP1.4. meeting, https://indico.cern.ch/event/979793/

[5.1] A. Himmerlich et al. "Defects formed in boron-doped Si diodes after high energy electron irradiation" 38th RD50 online Workshop 2021.

[5.2] Y. Gurimskaya et al. "Current Deep Level Transient Spectroscopy (I-DLTS) technique applied to p-type silicon diodes for Acceptor Removal Studies" 38th RD50 online Workshop 2021.

[5.3] C. Liao et al. „The boron-oxygen (BiOi) defect complex induced by irradiation with 6 MeV electrons in p-type silicon diodes" 38th RD50 online Workshop 2021.

[5.4] A. Himmerlich et al. "Defect characterization studies on highly irradiated Low Gain Avalanche Detectors" 39th RD50 Workshop 2021.

[5.5] C. Liao et al. "Investigation of the BiOi defect in EPI and Cz silicon diodes using Thermally Stimulated current (TSC) and Thermally Stimulated Capacitance (TS-Cap)" 39th RD50 Workshop 2021.

[5.6] A. Himmerlich et al. "Defect spectrocopy studies on irradiated LGADs" 17th Trento Workshop 2022.

[5.7] C. Liao et al. "The boron-oxygen (BiOi) defect complex induced by irradiation with 23 GeV protons in p-type epitaxial silicon diodes" IEEE Transactions on Nuclear Science, doi: 10.1109/TNS.2022.3148030

[6.2] E. Curras. "Low Gain Avalanche Detectors for 4-dimensional Tracking Applications in Severe Radiation Environments". Proceedings of the 29th International Workshop on Vertex Detectors (VERTEX2020), JPS Conf. Proc. 34, 2021, https://doi.org/10.7566/JPSCP.34.010015

[6.3] E. Curras, M. Fernandez, M. Moll, «Gain reduction mechanism observed in low gain avalanche diodes», NIMA (2022) 166530 https://doi.org/10.1016/j.nima.2022.166530

[6.4] M. Jiménez-Ramos, et al., «Study of Ionization Charge Density-Induced Gain Suppression in LGADs» Sensors 22 (3) s22031080, https://doi.org/10.3390/s22031080

[6.5] E. Curras, et al., «Gain suppression mechanism observed in Low Gain Avalanche Detectors» 16th Trento Workshop on Advanced Silicon Radiation Detectors, Feb, 2021
[6.6] M. Fernandez, et al., «Status report on the radiation tolerance assessment of CNM AIDA2020v2 and HPK-P2 LGADs», 16th Trento Workshop on Advanced Silicon Radiation Detectors, Feb, 2021
[6.7] E. Curras, et al., «Gain suppression mechanism observed in Low Gain Avalanche Detectors» The 38th RD50 Workshop, Jun, 2021
[6.8] E. Curras., «LGADs for timing applications in high energy physics» EP R&D seminar, Dec, 2021
[7.1] EP-DT Training Seminar (Virtual), April 28 2021: Finite-element transient Monte Carlo simulations for the optimisation and better understanding of silicon sensor prototypes
[7.4] 2nd Allpix Squared User Workshop (Virtual) August 18 2021 : Transient simulations of monolithic small collection diode CMOS sensors in Allpix Squared
[7.5] 9th Beam Telescopes and Test Beams Workshop (Virtual), Feb 9 2021: Test-beam and simulation studies of the monolithic CMOS silicon sensor CLICTD
[7.6] 2nd Allpix Squared User Workshop, https://indico.cern.ch/event/1043567/
[7.7] Test-beam and simulation studies for the CLICTD technology demonstrator - a monolithic CMOS pixel sensor with a small collection diode, Submitted to JPS Conf. Proc., arXiv:2106.12925
[7.8] Transient Monte Carlo Simulations for the Optimisation and Characterisation of Monolithic Silicon Sensors; NIMA (2022) 166491, https://doi.org/10.1016/j.nima.2022.166491

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[6.2] R. Heller, Systematic study of heavily irradiated LGAD stability using the Fermilab Test Beam Facility. The 38th RD50 Workshop, CERN. Jun, 2021.
[7.2] D. Dannheim et al., Combining TCAD and Monte Carlo methods to simulate CMOS pixel sensors with a small collection electrode using the Allpix2 framework, NIMA964, 2020, 163784
[7.3] Garfield++, https://garfieldpp.web.cern.ch/garfieldpp/

WP2 Gas Detectors

1. Introduction

Gas based detectors are key technologies for radiation detection in particle physics experiments. They provide excellent performances for large area, low mass and radiation hard, relatively cheap and rather easy-to-build detector solutions. They can have large dynamic range, stand rates above MHz/cm^2, achieve space resolution below 100μm as well as sub-ns time resolutions, good energy resolution and cluster counting capabilities.

WP2 focuses on large area detection systems, novel technological solutions and a flexible R&D support framework of scientists, tools and infrastructures to support new and emerging research activities. They are lined up with the ECFA Detector Research and Development Roadmap [17] matching recommendations in Section 1.3 concerning key technologies. These include large area integration, high rate, precise timing and discharge quenching capabilities as well as common challenges such as gas mixture optimizations including eco-friendly mixtures, development of robust photocathodes, dedicated front-end electronics, alternative readout methods and development tools in the fields of electronics and software to strengthen R&D frameworks.

The WP2 activities are embedded in the EP-DT-DD Gas Detector Development (GDD) team and in the EP-DT-FS gas group. In 2021, the EP-RD programme has funded two Fellows and two Doctoral students (15 months), one technical student (3 months) and two trainees (6 months). The Gentner doctoral programme has supported two projects on front-end electronics and tracking systems based on Micro Pattern Gas Detectors (MPGDs). The WP2 activities use synergies with the AIDAinnova project on eco-friendly gas mixture studies (AIDAinnova WP7, Gaseous Detector), which are integrated into the CERN Environmental Protection Steering (CEPS) board, and on the development of common data acquisition systems (AIDAinnova WP3, Test beam and DAQ infrastructure). The CERN Quantum Technology Initiative (QTI) is funding a doctoral project on the implementation of new materials in gaseous detectors. The WP2 activities are carried out in cooperation with the international RD51 collaboration, creating synergies in the research programme and in the use of the available facilities.

2. Main activities and achievements in 2021

The main activities and achievements of WP2 Gas Detectors in 2021 are reported in the following sections. Ongoing research on gaseous detectors with precise timing, with a focus on large area PICOSEC Micromegas, is outlined in the section 2.1. Section 2.2 describes the modelling and simulation of the signal induction with resistive electrodes. The activities on the VMM3a front-end of the RD51 Scalable Readout System (SRS) are presented in the section 2.3. A MPGD-based tracking system for future experiments is reported in section 2.4. Section 2.5 is a description of scintillation light readout of MPGDs. The research on graphene-based functional structures and nanostructures for novel gaseous detectors is presented in section 2.6. Finally, section 2.7 highlights the achievements of studies on eco-friendly gases for RPC detectors operating at LHC-like background conditions.

2.1. Large area PICOSEC Micromegas

(F. Brunbauer, D. Janssens , M. Lisowska, A. Utrobičić)

The PICOSEC Micromegas (MM) detector is a gaseous detector with precise timing based on a Cherenkov radiator coupled to a semi-transparent photocathode and a MM amplifying structure as shown in Fig. 1. Time resolutions better than 25 ps for Minimum Ionizing Particles (MIPs)_ have been measured on a single channel prototype with 1 cm^2 active area [18]. Ongoing developments are focused on scaling up both active area and number of channels. Achieving this aim depends on the capability of preserving time resolution when the signal is shared between different channels and on having uniform response over the full area. To this aim, a new prototype with 100 channels and an active area of 10x10 cm^2 was designed. It is 100 times larger than the first single-channel prototype and 10 times larger than the first multi-pad device [19]. The uniformity in the response calls for a planarity better than 10 µm for the 200 µm pre-amplification gap over the full active area. This requirement has been satisfied using a polished Micromegas PCB with a rigid ceramic core from the CERN MPT workshop and by removing all mechanical stresses in the detector assembly that would have affected the planarity of the PCB and radiator crystal.

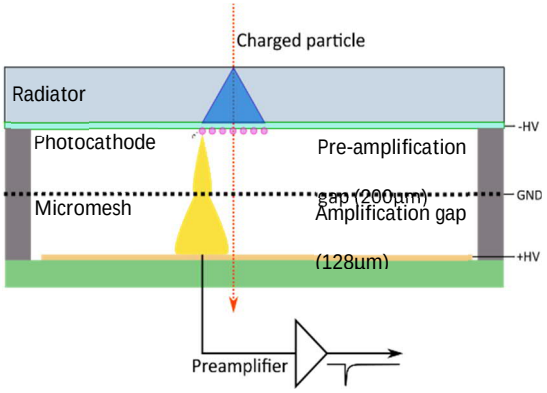

Fig. 1: PICOSEC Micromegas detector concept.

Two of these detectors have been built, equipped with Cesium Iodide (CsI) and Diamond-Like Carbon (DLC) photocathodes, tested in the laboratory and successfully operated with 80 GeV muon beams at the SPS H4 test beam, see Fig. 2 [1-3]. Preliminary results with the CsI photocathode show a time resolution below 25 ps for all measured pads [4] in agreement with the results from the 1 cm^2 single channel prototype, see Fig 2b. Signal arrival time has a similar dependence on the electron peak charge for all measured pads along a horizontal row indicating a uniform pre-amplification gap thickness as shown in Fig. 2c [20]. Preliminary analysis shows that a time resolution of 30 ps can be achieved for signals shared between 4 neighbouring pads suggesting that the time performance is not significantly degraded by the readout segmentation. Additionally, a large area 10x10 cm^2 DLC photocathode was investigated to find a robust solution against ion bombardment. Measurements on the prototype with the DLC photocathode resulted in a time resolution below 45 ps for all measured pads [4].

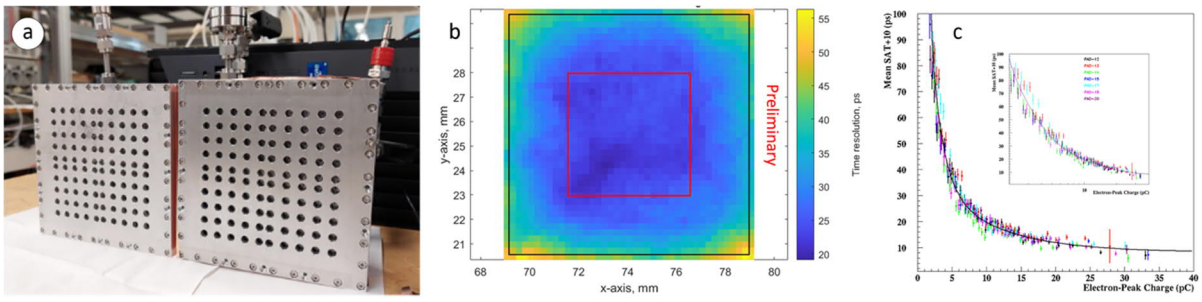

Fig. 2: a: Two 100 cm^2 PICOSEC Micromegas detector prototypes operated in SPS H4 test beams. b: Time resolution map within a 1 x 1 cm^2 pad. c: Signal arrival time vs. electron peak charge for pads on horizontal row [20].

In addition to tileable modules, optimization studies of 1 cm^2 single-channel prototypes were carried out. As expected from modelling, a prototype with a thin pre-amplification gap of 120 μm produced at CEA Saclay displayed excellent time resolution below 20 ps. A resistive MM with DLC photocathode, aiming at improving detector robustness and stability, showed a time resolution below 40 ps [4-5] for the standard gap configuration. These design features will be implemented in the next prototype with 100 channels 100 cm^2 active area to further improve its timing performance. Current detectors are read out using commercial high-bandwidth amplifiers and oscilloscopes. This readout chain is not scalable to high channel counts. To develop an alternative readout chain compatible with several hundreds of channels, various implementations of custom discrete amplifier circuits have been tested. Scalable high-bandwidth amplifier cards developed at CEA Saclay which were mounted on a multi-channel PICOSEC MM during a test beam are shown in Fig. 3. Preliminary results are showing promising timing performances, although they are not yet at the level of results obtained with the commercial amplifiers. In addition to custom amplifier developments, the multi-channel SAMPIC Waveform TDC has been used to digitize the signals and a good preservation of timing performance has been demonstrated for the available sampling rates of 6.4 and 8.5 GS/s. Other readout methods including alternative discrete circuits and ASIC-based solutions are under investigations.

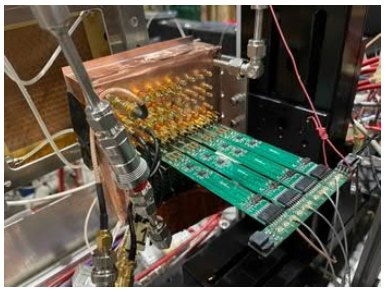

Fig. 3: Custom preamplifier cards on one PICOSEC Micromegas 100 channels module.

2.2. Modelling and simulation: signal induction with resistive electrodes

(D. Janssens)

For detectors with resistive elements, the time dependence of the signals is not solely driven by the movement of the charges in the drift medium but also by the time-dependent reaction of the resistive materials. In such geometries, the weighting potential becomes dynamic due to the medium's finite conductivity [21-23]. Since these potentials can only be obtained analytically for a small subset of the large group of existing detectors, a numerical method is used for modelling the time dependence of signals in resistive detectors. COMSOL Multiphysics provides such time-dependent solutions and in conjunction with Garfield++ allows for targeting the microscopic modelling of the signal induction in this class of detectors.

Following the successful implementation of a reformulated version of the extension to the Ramo-Shockley theorem, which is more suitable for numerical models, into Garfield++, it is now being applied to a wide range of resistive detectors. An example of a geometry leveraging the effect of resistive materials is the two-dimensional interpolation anode structure, initially developed for the MicoCAT detector [24]. This is shown in a schematic representation in Fig. 4a. A comparison was made between our results and the measurements and RC-circuit based modelling performed by H. Wagner et al. [25] on the distortion caused by linear interpolation found on the edge of a cell [6]. The result is given in Fig. 4b, where both models capture the increase in distortion as the charges are deposited further away from the readout node. Staying within the family of MPGDs, a resistive plane Micromegas and PICOSEC Micromegas detectors are also being simulated to study the impact of a resistive layer on timing and spatial performance. Outside this class of devices, we are looking at Multigap Resistive Plate Chambers (RPC) and solid-state detectors such as AC-coupled Low Gain Avalanche Detectors (AC-LGADs) and 3D diamond detectors [6]. For the latter two, measurements are available from the groups of N. Cartiglia and G. Passaleva, respectively, which will serve as a reference to the simulations.

Additional detector technologies including µRWELL and resistive strip Micromegas will be added to the list of investigated detector models and will be accompanied with experimental measurements in the GDD laboratory currently being prepared.

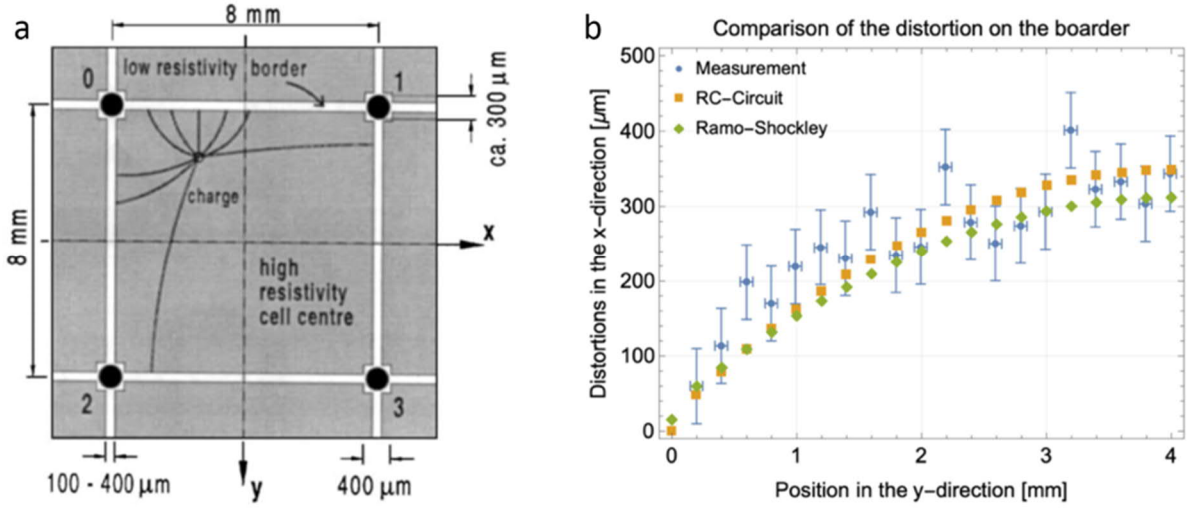

Fig. 4: The two-dimensional interpolation readout uses a linear interpolation algorithm to retrieve the position of the charge deposition; a: Schematic illustration of a single cell within the resistive anodes; b: Comparison of the simulated weighting potential distortion of the low resistivity boundary of a cell and the data found in H. Wagner's work.

2.3. VMM3a front-end of the RD51 Scalable Readout System

(L. Scharenberg)

The BNL/ATLAS VMM3a front-end ASIC offers, among other advantages, acquisition rates in the MHz regime and compatibility with various detector technologies due to an adjustable electronics gain and a variation of input capacitance over several hundreds of pF. The integration of this front-end into the RD51 SRS [26] offers the possibility to adapt from small laboratory setups to large readout systems and take advantage of the novel features of this front-end ASIC.

In 2021 the VMM3a/SRS data acquisition rate was improved from tens of Mbps to 356 Mbps per readout ASIC [7]. The most significant improvement was achieved by firmware changes on the data transmission. The clock speed and stability for the data transfer from the ASIC was optimised, including a dedicated matching for the data transmission between front-end board and concentrator cards. In Fig. 5, an X-ray radiography made up of 277 x 10^6 X-ray photons recorded in 180 s is shown.

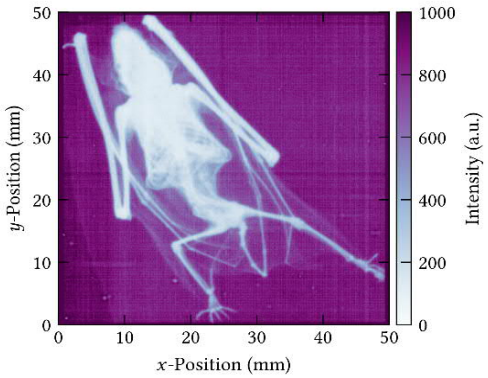

Fig. 5: X-ray image of a bat (1.5 MHz cluster rate) [7].

In parallel to optimisations of readout rate and data transmission, the scalability of the system was tested by equipping a tracking and timing telescope during the 2021 RD51 beam tests at the SPS H4 extraction line. While previously working with single detector setups for X-ray imaging, a larger system of five detectors and more than 2.5k readout channels allowed for commissioning and optimisation of the power distribution, grounding scheme, as well as the synchronisation between detectors. During the beam tests, triple-GEM and straw tube detectors were characterised and an interface to PMT and coincidence signals (NIM) was set up for additional timing purposes.

The continuous high-rate self-triggered readout allowed for recording single-particle tracks for rates of up to 1 MHz per beam spill. The significant reduction in the data acquisition time for each test setting allowed for the fast reconstruction of SPS beam extraction profiles, as shown in Fig. 6. The tracking and timing system allowed for characterising detector and electronics performances to the level of about 50 µm spatial resolution and 1 ns time resolution. The next steps will investigate the various ASIC settings to optimise the detector readout and further improve the achievable resolutions in energy, space and time.

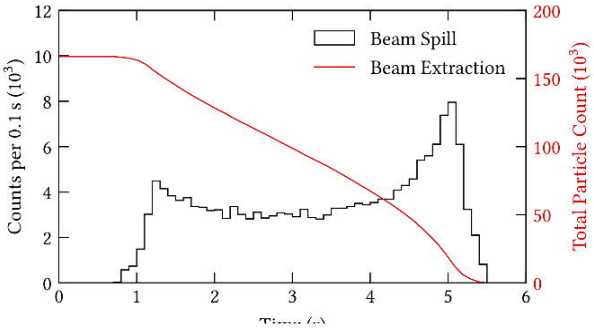

Fig. 6: VMM3a-based reconstruction of the spill structure (black) and of the particle intensity in the SPS machine (red) which is in agreement with the measurements by standard SPS beam monitors.

The activities have been carried out in connection with the developments of the RD51 collaboration and within the context of Gentner Doctoral Student scholarships [8-11]. The developments on the rate capability were achieved in strong collaboration with the European Spallation Source (ESS) and Bonn University. The activities on the beam telescope are also covered by task 3.5.2 of the AIDAinnova WP3.

2.4. MPGD-based tracking system for future experiments

(K. Floethner)

Future tracking detectors will have to operate in demanding environments with high signal and background rates. New detector technologies and readout solutions enabled by technological advances in MPGD manufacturing techniques are being explored to overcome these challenging requirements. A novel three-coordinate readout approach is being explored to resolve ambiguities and enable higher rate capabilities as well as to improve position resolution. Following an optimisation of geometrical parameters for the XYV readout with simulations, a detector readout plane was designed and production tests are ongoing, as shown in Fig. 7.

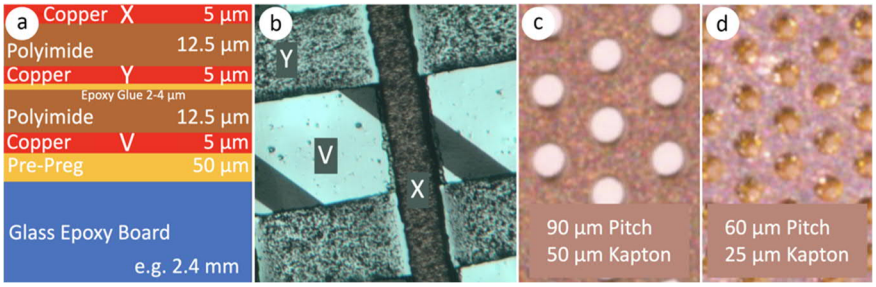

Fig. 7: a: Schematic cross-section for three-layer readout. b: Microscopic image of a production test realized at the CERN MPT workshop: pitch and width in µm X/Y/V: 400/400/~283, 80/180/220. c, d: Microscopic images of small- pitch foils.

In order to study the impact on space resolution, signal saturation and detector stability, GEM foils with smaller pitch are under investigation. Depending on the position in the GEM stack, a small pitch GEM could improve the spatial resolution, the intrinsic signal saturation or the discharge probability. The GEM foils shown in Fig. 7c have been tested and successfully operated at the SPS test beam as first element of a triple-GEM. Additional laboratory tests with soft X-rays and alpha sources, as well as beam studies will be performed along with a comparison with simulations.

2.5. Scintillation light readout of MPGDs

(F. Brunbauer)

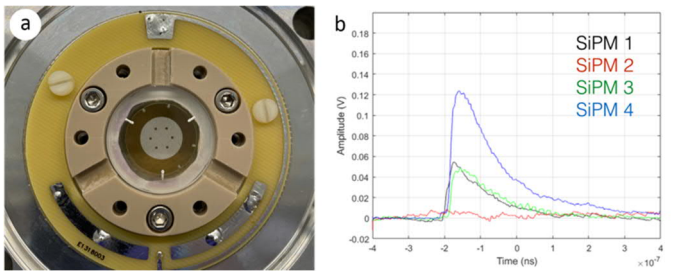

Fig. 8: a: 1 cm diameter optical Micromegas on sapphire substrate. b: Signals of SiPMs arranged in a 2x2 array recording scintillation light emitted in a MIP event.

Scintillation light emitted during avalanche multiplication in MPGDs can be recorded with pixelated imaging sensors and sensitive fast photon detectors. SiPMs are attractive for the optical readout of MPGDs due to their high sensitivity, time resolution and the possibility to arrange them in arrays for spatial reconstruction. To explore the potential of SiPMs for spatial reconstruction and timing, a Micromegas detector integrated on a sapphire substrate with a semi-transparent indium tin oxide (ITO) anode was developed, see Fig. 8a. A Cherenkov radiator coated with a semi-transparent CsI photocathode was used to create primary electrons. Single SiPMs or 2x2 arrays of SiPMs were placed in contact with the substrate to record the scintillation light emitted in the Micromegas amplification region. The detector was characterized in muon beams in the SPS H4 beam line. An exemplary muon event is shown in Fig. 8b, where the signal is shared across four 4x4 mm^2 SiPMs in a 2x2 array. The relative intensity of individual pixels was used to reconstruct the hit location of incident particles. The results were compared with reconstructed trajectories from a tracker. Good agreement between reconstructed position and predicted hit location was found although improved reconstruction algorithms are needed and additional SiPM pixels may offer better precision for shared signals.

2.6. Graphene-based functional structures and nanostructures for novel gaseous detectors

(G. Orlandini)

Low-dimensional materials and nanostructures may allow detailed tailoring of microscopic transport processes in MPGDs and could offer novel charge production methods. A doctoral project funded by the CERN Quantum Technology Initiative (QTI) started at the end of 2021 and aims at exploring the potential of nanomaterials for MPGDs including their use as conversion layers for radiation detectors, potentially offering increased quantum yield as well as wider sensitivity to incident radiation energies and types. Coating of photocathodes with 2D materials can enhance their lifetime by protecting them from environmental conditions such as humidity or ion bombardment. In addition, a modification of the surface work function may increase the quantum efficiency of the photocathodes. In addition to studies of nanomaterials for primary charge production, they may also be used to control charge transport processes in MPGDs. The different transparency for electrons and ions through low-dimensional materials such as graphene may be exploited for optimizing the operation of gaseous detectors. While permitting electrons to pass through the layer and to be transferred to amplification stages, these layers may block ions and thus reduce field distortions due to the accumulation of ions in large drift volumes. In addition, ion-feedback processes and photocathode damages induced by ions may be suppressed.

2.7. Studies on eco-friendly gases for RPC detector in LHC-like background conditions

(M. Corbetta, B. Mandelli, G. Rigoletti, M. Verzeroli)

In the framework of the strategies adopted by CERN to reduce GreenHouse Gas (GHG) emissions from particle detectors, several studies are ongoing to search for alternatives gases to $C_2H_2F_4$ (R-134a) and SF_6, which are GHG emitters currently used in RPC detectors [12-16]. Detector performances with eco-friendly gas mixtures are studied both in laboratory conditions with cosmic muons and at the CERN Gamma Irradiation Facility (GIF++) with a muon beam and gamma particle background, up to a rate of 600 Hz/cm^2, similar to the expected background rates of HL-LHC in the ATLAS and CMS barrel regions.

Fig. 9a shows the efficiency and streamer probability curves for the most relevant gas mixtures tested in the presence of the muon beam only. Fig. 9b shows the currents drawn by the RPC, evaluated at the detector working point, as a function of the gamma background rates at GIF++. The addition of up to 30-40% of CO_2 or He to the standard gas mixture reveals a detector performance comparable to the standard gas mixture, indicating a possible mid-term solution to reduce GHG emissions.

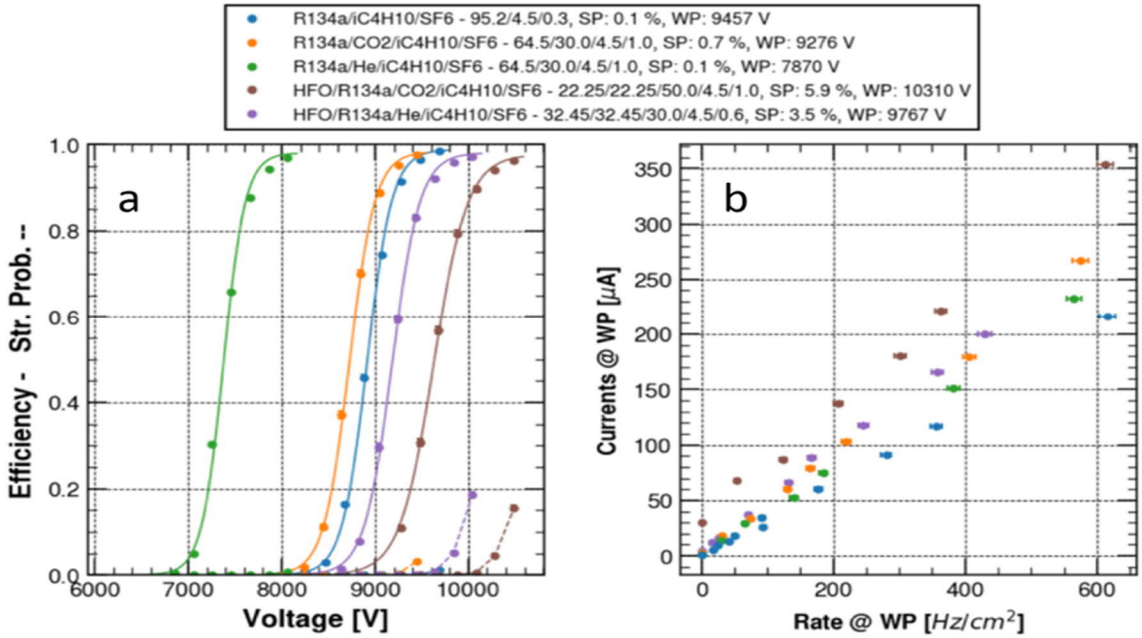

Fig. 9: a: Efficiency (continuous line) and streamer probability (dashed line) in presence of muon beam. b: Currents as a function of different gamma background rates for RPC operated with standard gas mixture and selected eco-friendly gas mixtures.

Gas mixtures based on the use of HFO1234ze with a small fraction of R134a and the addition of CO_2 or He have been tested to further lower the working point and the use of R134a. Preliminary results show a higher streamer probability that can be reduced by increasing the SF_6 concentration to 1%. In the presence of high gamma rates a larger efficiency drop is visible and the currents are about 75% higher with respect to the standard ATLAS and CMS gas mixture, a phenomenon probably due to the presence of HFO and a higher SF_6 concentration. This has to be studied more in detail for long-term operation.

In parallel, SF_6 alternatives have also been evaluated at GIF++, in particular Novec 4710 and Amolea 1224yd. A small concentration of both gases is enough to match the SF_6 performance especially in terms of streamer probability and detector currents. Further studies are necessary to evaluate possible chemical and radiation effects of these gases in the RPC gas mixture.

3. Publications and contributions to conferences and workshops

[1] A. Utrobičić, “Assembly and gain uniformity measurements of the new large area PICOSEC detector”, RD51 Mini-Week, 15-19 February 2021

[2] A. Utrobičić, “PICOSEC 2021 RD51 beam test”, RD51 Mini-Week, 15-19 February 2021

[3] A. Utrobičić, “PICOSEC update: improvements in gain uniformity of 100 channel prototype and single pad detector tests”, RD51 Collaboration Meeting, 14-18 June 2021

[4] A. Utrobičić, “PICOSEC precise timing detectors: recent results, status and plans”, RD51 Collaboration Meeting, 15-19 November 2021

[5] M. Lisowska, “Precise Timing with PICOSEC Micromegas Oct 2021 RD51 beam test campaign”, RD51 Collaboration Meeting, 15-19 November 2021

[6] D. Janssens, “Modeling of signal formation in detectors with resistive elements: contribution of material specific conductivity”, RD51 Collaboration Meeting, 14-18 June 2021

[7] L. Scharenberg et al., “Rate-capability of the VMM3a front-end in the RD51 Scalable Readout System”, Accepted for publication in NIM A

[8] L. Scharenberg et al., “A simple method to improve the position resolution”, Spring Meeting of the German Physical Society (DPG-Frühjahrstagung), 15–19 March 2021, Technical University of Dortmund, Dortmund, Germany (virtual meeting).

[9] L. Scharenberg et al., “Position reconstruction studies with GEM detectors and the charge-sensitive VMM3a ASIC”, 12th International Conference on Position Sensitive Detectors (PSD12), 12–17 September 2021, University of Birmingham, Birmingham, United Kingdom (poster presentation)

[10] L. Scharenberg, “Exploring Next-Generation Readout Electronics for MPGDs”, 7th EIROforum School on Instrumentation, 07–11 June 2021, Institut Laue-Langevin (ILL), Grenoble, France (virtual meeting, video presentation).

[11] L. Scharenberg, “Developing a general-purpose readout system for gaseous detectors”, CERN EP-DT Training Seminar, 08 December 2021, CERN, Geneva, Switzerland

[12] M. Corbetta, R. Guida, B. Mandelli, "Studies on fluorine-based impurity production in Triple-GEM detectors operated with CF4-based gas mixture", NIM A 1004 (2021) 165373

[13] B. Mandelli, R. Guida, G. Rigoletti, "Performance studies of RPC detectors operated with new environmentally friendly gas mixtures in presence of LHC-like radiation background", PoS 2021 (ICHEP2020) 857

[14] G. Rigoletti, R. Guida, B. Mandelli “Performance studies on RPC detectors operated with low Global Warming Potential gases”, 2021 IEEE NSS MIC

[15] M. Corbetta, R. Guida, B. Mandelli, G. Rigoletti, “Studies on impurities and F-radicals production in gaseous detectors operated with Freon based gas mixtures at LHC Experiments”, TIPP 2021

[16] G. Rigoletti, R. Guida, B. Mandelli “Studies on RPC operation with low GWP gases”, Mini-Workshop on gas transport parameters for present and future generation of experiment

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[17] ECFA/RC/21/510, CERN-ESU-017, DOI: 10.17181/CERN.XDPL.W2EX

[18] J.Bortfeldt et al., "PICOSEC: Charged particle timing at sub-25 picosecond precision with a Micromegas based detector", NIM A 903 (2018) 317-325

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[20] A. Kallitsopoulou, "Development of a simulation model and precise timing techniques for PICOSEC-Micromegas detectors", Master's Thesis (2021)

[21] W. Riegler, "Induced signals in resistive plate chambers", NIM A 491 (2002) 258- 271

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[23] W. Riegler, "An application of extensions of the Ramo-Shockley theorem to signals in silicon sensors", NIM A 940 (2019) 453-461

[24] A. Orthen et al., "Recent progress with the MicroCAT gaseous imaging detector", NIM A 478 (2002) 200-204

[25] H. Wagner et al., "On the dynamic two-dimensional charge diffusion of the interpolating readout structure employed in the MicroCAT detector", NIM A 482 (2019) 334-346

[26] M. Lupberger et al., "Implementation of the VMM ASIC in the Scalable Readout System", NIM A 903 (2018) 91-98

WP3.1 R&D on Noble-Liquid Calorimetry

(Summary prepared by B. Francois, M. Barba, M. Aleksa)

1. Introduction

The next generation of calorimeters for future colliders will have to provide very good energy resolution and high granularity, as well as a strong control over the systematic uncertainties and acceptance. Noble-Liquid Calorimetry can be optimised to meet these requirements and has been proposed for an FCC-ee experiment [1] as well as for FCC-hh [2]. This work package deals with two challenges of this technique and is therefore organized around these two activities: the design of a new type of highly-granular readout electrode realized as multi-layer PCBs and the development of new high-density feedthroughs.

Currently two fellows are working for WP3.1: one entirely funded by the EP R&D program; the second fellow shared equally between EP R&D and funds from CERN CryoLab. During summer 2021 two summer students contributed to the effort. EP R&D WP3.1 is the core of a small international collaboration working on noble-liquid calorimeters for future collider experiments, which is partly funded by AIDAinnova WP8. Monthly group meetings are organised to discuss the progress [3].

2. Main activities and achievements in 2021

2.1. Readout electrode design

The detector granularity targeted within this R&D project is a factor 10 to 15 higher than in the ATLAS Liquid Argon calorimeter [4], reaching a typical (strip) cell size of 2 (0.5) x 1.8 x 3 cm^3 in the polar, azimuthal and radial directions, respectively. Read-out electronics sitting outside the cryostat is currently studied as a baseline, but alternatives using cold electronics are also considered. Since precision measurements of photons down to 300 MeV will require an excellent control of the electronic noise, the signal extraction through the read-out electrodes and cables before reaching the first amplification step outside the cryostat, is one of the biggest challenges and needs careful optimisation. It is required to keep the crosstalk at the percent level and the noise at values significantly below the ionization signal of a Minimum Ionizing Particles (MIP).

A 7-layer PCB readout electrode with 12 longitudinal segments has been implemented in finite-element software (ANSYS®) to perform detailed signal simulations. Figure 1 shows the crosstalk that was derived[7] by injecting a triangular current pulse on cell 7 (numbering scheme can be seen in the middle of the figure) and comparing the peak-to-peak current values between this cell and its neighbours. Note that the signal trace of cell 7 passes below cell 6, then between cells 4 and 5, and finally below cell 1 to reach the edge of the electrode. The crosstalk signals for typical cells in a PCB without a ground shield surrounding the signal traces shown on 1 (right), is a maximum of 12%. This number drops to 2% when adding ground shields above and below the signal traces. In this scenario, the crosstalk for neighbouring cells in the strip layer is of the order of 6%, which is similar to that achieved by ATLAS [5].

As shown in Figure 2, the noise as a function of the detector cell capacitance has been estimated based on a detailed analytical implementation of the whole readout chain (transmission line, coax cables, pre-amplifier and shaper). The detector cell capacitance shown in Figure 2, as obtained from the finite-element study, allows us to derive the noise value per cell. Since a MIP deposits an energy per cell (here two double-gaps) leading to a charge signal of about 30000e^-, it can be seen that a signal-to-

[7] Neglecting the resistive crosstalk and without simulating the front-end electronics

noise ratio above 5 can be achieved for MIPs, allowing us to track single charged particles in the calorimeter.

Currently a PCB prototype is being produced by the CERN EP-DT PCB laboratory.

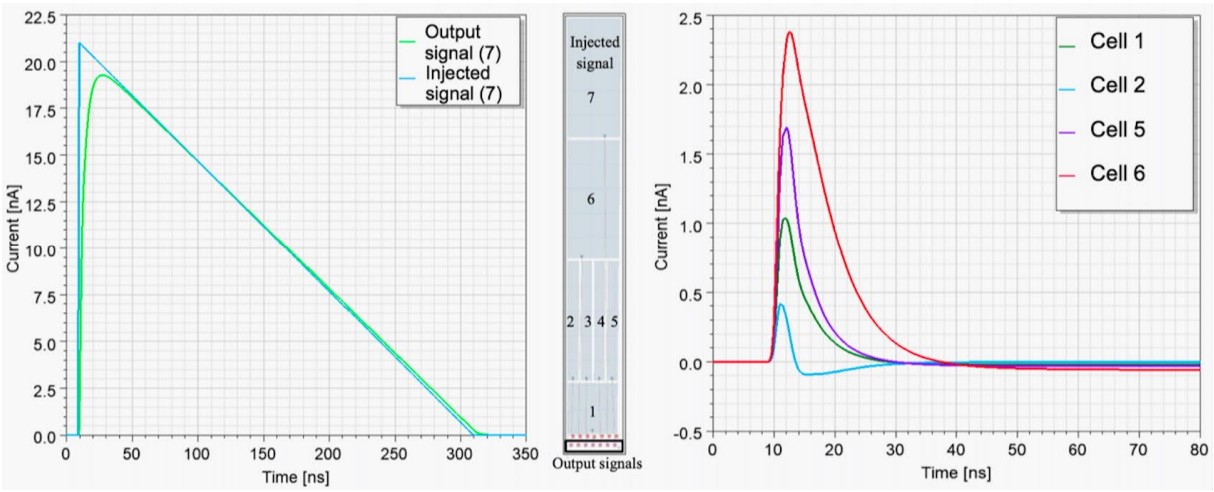

Figure 1: Cross talk simulations using ANSYS® without any shaping applied. Left: Injected typical triangular ionization pulse in cell 7 and the signal read on the output board. Middle: Numbering scheme of the read-out cells. Right: Crosstalk signals in neighboring cells. Note, that the y-axis has a different scale on both plots.

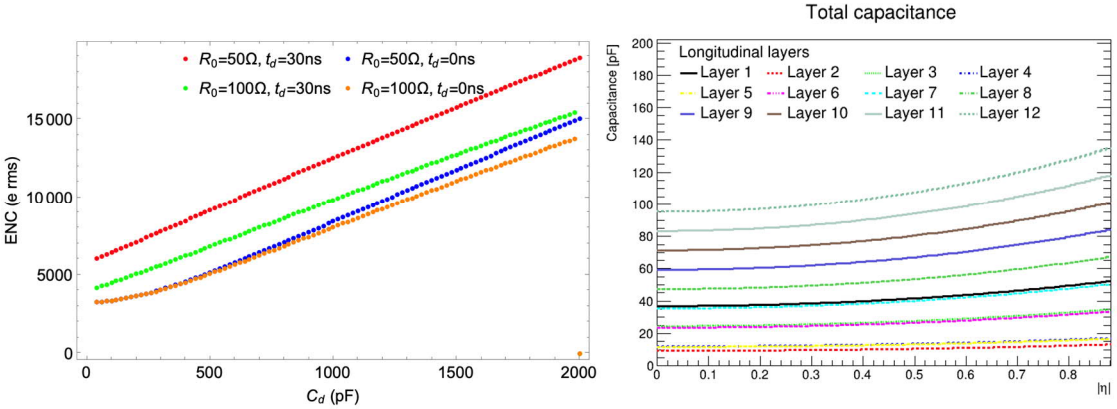

Figure 2: Left: equivalent noise charge as a function of the cell capacitance for different signal extraction schemes and for a charge pre-amplifier with e_n=0.5 nV/√Hz and i_n = 1 pA/√Hz and a shaping time of 200 ns. Right: cell capacitance as a function of pseudo-rapidity for each longitudinal segment (layer).

2.2. High-density signal feedthroughs

Another important challenge of the high granularity is the extraction of the numerous signal channels to the outside of the cryostat where the electronic boards will amplify and further process the induced detector signals. R&D activities focusing on the development of new connector-less feedthroughs are ongoing. As shown below, a concept was developed for realising high-density flanges, allowing up to 20000 signal wires to pass per feedthrough.

The geometry of a single feedthrough flange is presented in Figure 3. It consists of a stainless-steel grid with fiberglass structures with small slits, allowing the cables to pass through. These slits are then filled with epo-tek glue, and the fiberglass structures are fixed to the body grid with a stainless-steel compression plate and an indium seal to ensure the leak-tightness.

An experimental setup, illustrated in Figure 3, has been conceived, allowing simultaneous pressure and leak tests to be performed at low temperature. Figure 4 shows stainless steel samples (left) and G11 samples (right) with the epo-tek glue applied. The small samples that have been tested were arranged into an array to a complete feedthrough flange supported by a stainless steel structure as shown in Figure 5 5. To validate the concept, numerous tests have been performed below 87 K and at 3.5 bar showing a leak-rate of 10^{-9} mbar l/s.

Furthermore, four different designs of flanges have been studied, analysing the mechanical stress under 3.5 bar of pressure at room temperature and cryogenic temperature. An example of a flange design and its maximal deflection is illustrated in Figure 5.

The results of these tests are being summarised for publication in JINST.

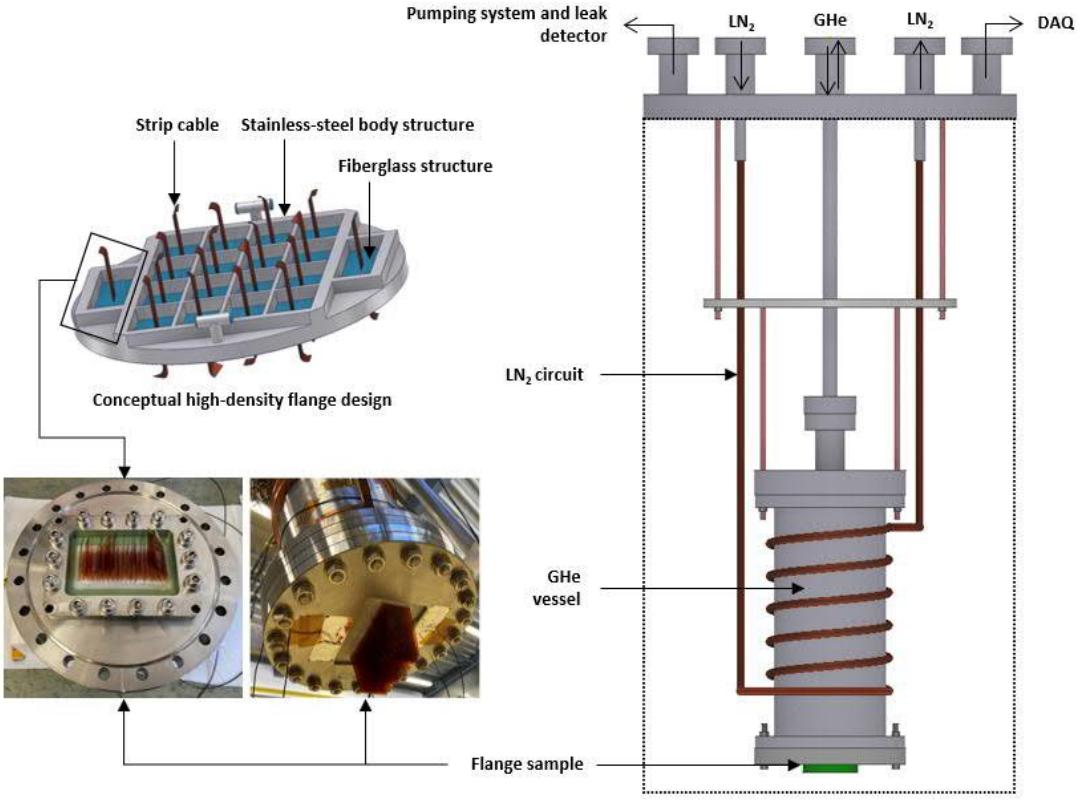

Figure 3: Left: Schematic illustration of the experimental setup and a flange sample. Right: Schematics of the test set-up.

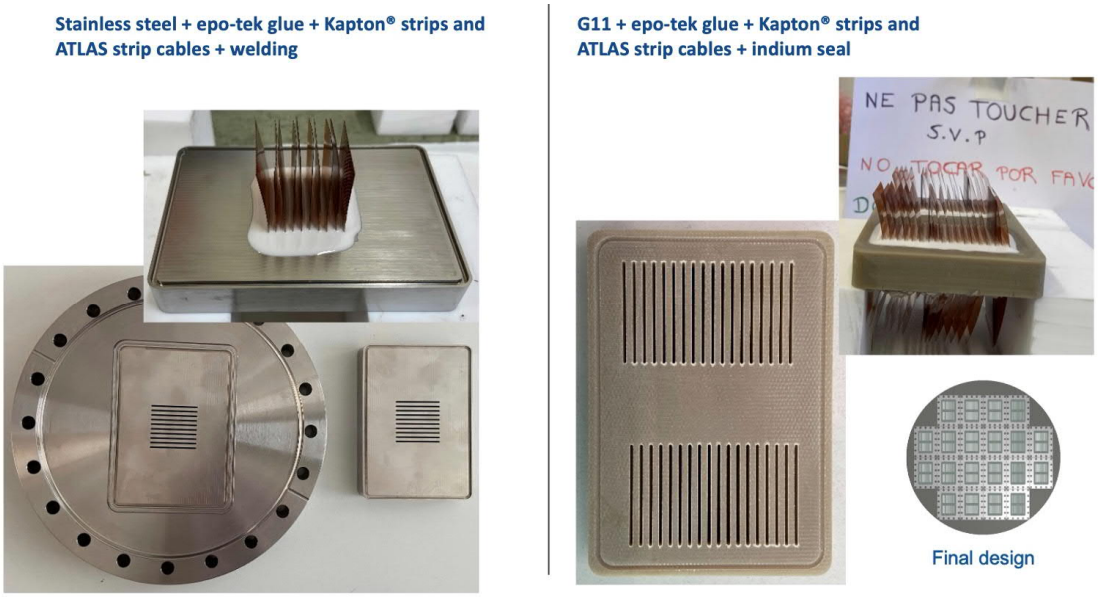

Figure 4: Pictures of feedthrough test samples with stainless steel (left) and G11 (right).

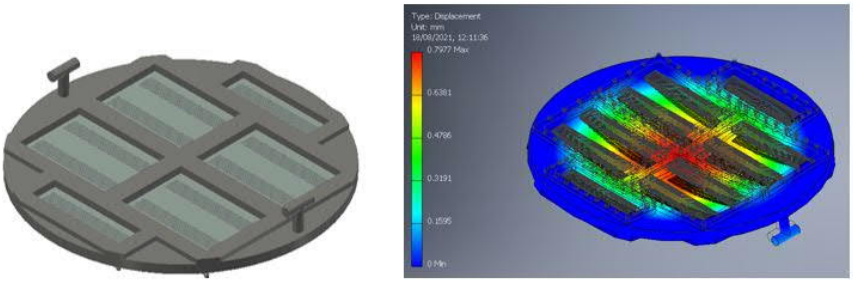

Figure 5: Schematic illustration of one of the four final flange designs studied and its maximal deflection at 3.5 bar

2.3. Full simulation performance studies

A complete and accurate FCC-ee detector description shown on the left side of Figure 6 has been implemented into the Key4HEP Full Simulation framework [6]. Detector performance studies with electrons and photons have been carried out indicating that a sampling term of the order of 8% can be achieved with 1.8 mm Lead absorbers, 1.2 mm LAr gaps and 12 longitudinal segments (see Figure 6 right). The same framework allowed us to study different combinations of absorbers (Lead or Tungsten) and/or Noble Liquids (LAr, LKr or LXe), showing that a sampling term of 7% could be achieved by replacing LAr with LKr (keeping the same layout as in the baseline scenario). It was shown that a sampling term of 2% could be achieved by completely removing the absorbers and hence approaching the case of a homogeneous calorimeter. Unfortunately this would enlarge the required depth considerably, excluding this solution for collider experiments [7].

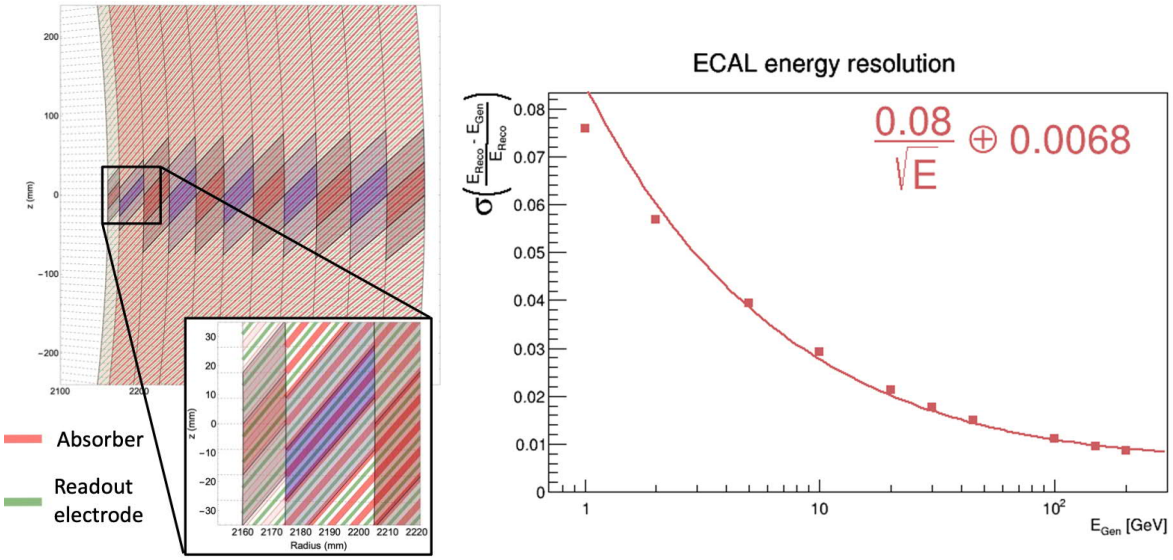

Figure 6: Left: Close-up view of FCC-ee detector geometry as implemented in the Key4HEP framework. The coloured parallelograms symbolise a possible summation of double drift gaps into read-out cells. Right: relative electron energy resolution as a function of the generated particle gun energy for the baseline detector scenario.

3. Publications and contributions to conferences and workshops

Presentations, reports, publications:

- B. Francois: Plenary talk 'Future Noble Liquid Systems' at the ECFA Detector R&D RoadMap Symposium of Task Force 6 Calorimetry (May 7, 2021), https://indico.cern.ch/event/999820/#4-future-noble-liquid-systems
- M. Waterlaat, B. Francois: CERN-STUDENTS-Note-2021-116, 'Performance study for different geometries of the future Noble Liquid calorimeter at FCC-ee', https://cds.cern.ch/record/2780060
- O. Reinicke, B. Francois: CERN Summer Student Report (https://cernbox.cern.ch/index.php/s/nGqHgw3wehWAePD)
- M. B. Higueras: Summary talk at the EP R&D Day in Nov. 2021, https://indico.cern.ch/event/1063927/
- B. Francois: Plenary talk 'Noble Liquid Calorimetry for a Future FCC-ee Experiment' at the FCC Physics Workshop (Feb 9, 2022), https://indico.cern.ch/event/1066234/contributions/4708987/
- B. Francois: Plenary talk 'Status of the FCC-ee LAr calorimeter software' at the FCC Physics Workshop (Feb 11, 2022), https://indico.cern.ch/event/1066234/contributions/4712003/
- B. Francois: Recorded presentation 'Noble Liquid calorimetry for a future FCC-ee experiment' at The 16th Vienna Conference on Instrumentation (Feb 21-25, 2022), https://indico.cern.ch/event/1044975/contributions/4663743/

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WP3.2 & WP3.2.1 R&D on SPACAL Calorimeter and Prospective R&D for Scintillator-Based Calorimeters

(Summary prepared by L. Martinazzoli, M. Pizzichemi, M. Salomoni, R. Calà, E. Auffray, P. Roloff, A. Schopper)

1. Introduction

The objective of WP3.2 is to develop a radiation-hard and cost-effective "spaghetti"-type sampling calorimeter. Targeting as a use-case the LHCb ECAL Upgrade II development, called "SPACAL", the performance requirements are: an energy resolution with a 10% sampling term and close to 1% constant term; a time resolution of the order of 20 ps above 20 GeV; radiation hardness up to 1 MGy for the innermost part of the calorimeter and 200 kGy for the region surrounding the innermost modules. Several active materials and geometries were investigated by means of experimental test benches and Monte Carlo simulations, as well as test-beam facilities both at CERN's SPS and DESY.
The objective of WP3.2.1 is to investigate fast and radiation-hard scintillating crystals for future detectors. Two lines of research have been pursued: one related to the materials to be used for the SPACAL prototype and, among the crystals studied, garnet crystals are the best candidate thanks to their cutting-edge radiation tolerance and timing properties. The second line focussed on the exploration of fast emission processes such as cross-luminescence, Cherenkov radiation, and innovative materials such as nanomaterials.
All WP3.2 and WP3.2.1 activities are being carried out in partnership with the Crystal Clear collaboration and LHCb member institutes (Barcelona University, Bologna University & INFN, MISiS Moscow, IHEP Protvino, Giessen University, FZU Prague, RINP Minsk). One fellow in EP-LBD, Matteo Salomoni, and a Ph.D. student (in EP-CMX-DA), Roberto Calà, are currently working on these work packages.

2. Main activities and achievements in 2021

2.1. R&D for scintillator based calorimetry

The characterization work on garnet (GAGG) crystals performed in 2021 identified samples able to reach state-of-the-art timing [1]. However, in the high-rate environment of the HL-LHC and future colliders, decay times of 50-60ns, as achieved currently by GAGG, can lead to significant spill-over of the light from one collision to the next, whilst light yields of 30000 photons/MeV or more could reduce the life expectancy of the photodetectors. In collaboration with the FZU institute (Prague), new GAGG compositions were developed, featuring much larger concentrations of Ce and Mg codopant, which lead to a strong reduction of the scintillation decay time at the expense of light yield. Several new samples were characterised by CERN, FZU, and Vilnius. They show a light output between 500 and

12000 photons/MeV and decay times from 1.7 ns to 25 ns. The results of this study have been summarised in a recently-submitted publication [2]. In spite of the light reduction, these samples showed competitive time resolutions, only 10% worse than the current state-of-the-art garnets. Monte Carlo simulations demonstrated that these new samples can suit the performance demands for the inner region of the SPACAL. R&D is ongoing to produce larger samples and to test their radiation tolerance in the next months.
In parallel, a characterization campaign of the scintillating properties of two sets of mixed BGSO (Bi4(GexSi1-x)3O12) crystals provided by ISMA (Ukraine) and FZU with Ge percentages ranging from 0 to 100% was performed. An optimum percentage, in terms of timing properties was reached for samples with Ge between 30% and 50%: a coincidence time resolution at 511 keV of 208 ± 2 ps was achieved for a 2×2×3 mm3 pixel with 40% Ge, while the smallest effective decay time of 50 ± 2 ns was obtained for a plate-shaped sample with 30% Ge.

The separation of the Cherenkov and scintillation light generated in a pure BSO sample was efficiently demonstrated using optical filters. Such a technique can be used in crystal-based dual-readout calorimetry applications, to improve the hadronic energy resolution compared to traditional methods. The results have been recently published in NIM A [3].

A set of BaF2 crystals doped with different amounts of yttrium, produced by the company SICCAS, was characterised to study both timing and scintillating properties as a function of the amount of dopant. High concentrations (10%) of Yttrium strongly suppress the slow emission component of BaF2, without degrading the ultra-fast component and therefore preserving the time resolution.

A test beam activity at CERN's SPS was performed in August 2021, in which the timing performance of ultrafast materials was measured for incident MIPs. The crystals characterized included LSO, BGSO, GAGG, Cherenkov radiators (PWO, TlCl), and nanomaterials (CdSe). Time resolutions as good as 20 ps were achieved with small pixels read-out by NINO electronics.

2.2. SPACAL Calorimeter simulation

The full Monte Carlo (MC) simulation framework developed in 2021 has been successfully employed to predict the performance of SPACAL modules (Tungsten absorbers with GAGG and Polystyrene fibres, and Lead absorber with Polystyrene fibres), with good agreement with respect to the energy resolution measurements carried out in recent beam tests.

The MC framework has been extended to include the possibility of simulating Shashlik modules, currently used in the LHCb ECAL. The Shashlik simulations have been validated against data from beam tests and ECAL operation in terms of energy resolution. The MC framework has been adapted to include the capability of simulating different cell granularities, readout options, and longitudinal segmentations. Detailed simulations of full ECAL configurations have therefore become possible, and several configurations representing the current ECAL geometry and the various upgrade proposals have been prepared and tested with input particle fluxes from the full simulation of the LHCb detector upstream of the ECAL.

Furthermore, the possibility to rotate the SPACAL modules around the pitch and yaw axes, in a full ECAL configuration, has been implemented into the full MC framework, and is currently under validation.

2.3. Beam tests @ DESY and CERN's SPS

A variety of prototypes has undergone extensive test campaigns with electrons at DESY, in the energy range 1 – 5.8 GeV, and at CERN up to 100 GeV. Figure 7 7 shows that a stochastic term of around

10%/√E is achieved with the Shashlik and the SPACAL W/GAGG and Pb/PS prototypes. As the example in the plot also shows, the performance of SPACAL worsens at small incidence angles due to differences in the sampling and longitudinal fluctuations depending on whether the particle first enters into a fibre or the absorber. To mitigate this effect, it is envisaged to orient the modules at an angle of a few degrees with respect to the LHCb beam axis. As a reference, Figure 7 8 also shows the performance of the Shashlik technology currently used in the LHCb ECAL.

The timing characteristics achieved at test beams with SPACAL Pb/PS and Shashlik prototypes are shown in Figure 8, in the energy range 2-100 GeV.

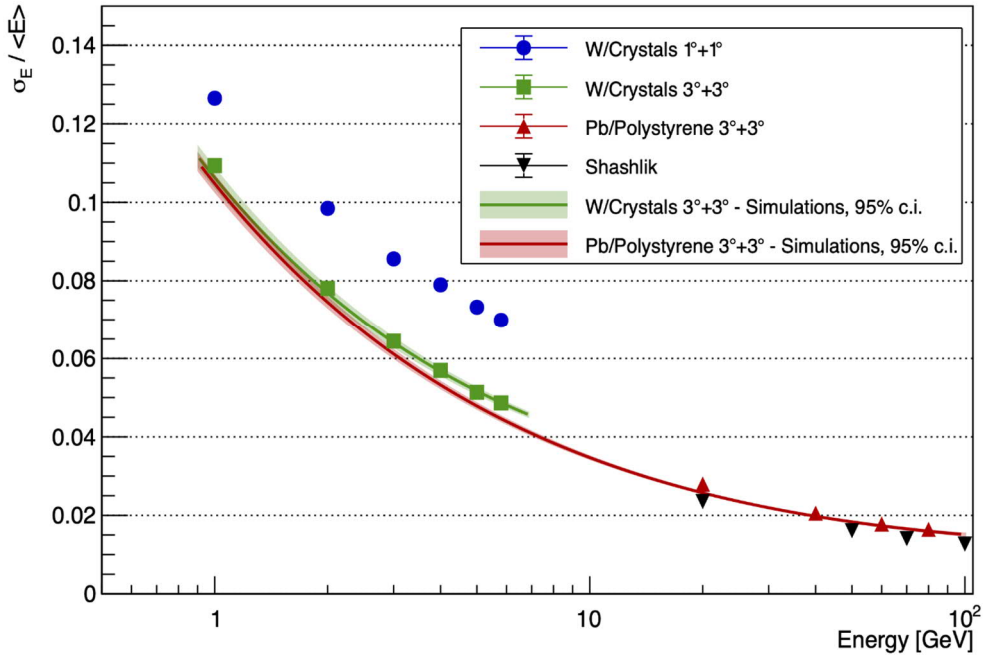

Figure 7: Energy resolution for SPACAL W/GAGG and Pb/PS prototype modules oriented at 3° + 3° with respect to the beam axis and for a Shashlik module, as measured in a test beam. For comparison, the energy resolution for a SPACAL W/GAGG prototype module oriented at 1° + 1° with respect to the beam axis is also shown.

All the measurements were performed with a Hamamatsu photomultiplier tube (PMT) of type R7600-U20, with direct optical coupling between the sample and PMT. The measured time resolution above 30 GeV is about 15 ps for both SPACAL and Shashlik designs. Very similar time resolutions were observed for the SPACAL W/GAGG option. Adding a light guide to SPACAL degrades the time resolution by a few picoseconds but preliminary tests suggest that introducing an optical coupling between the light guide and fibres can reduce the performance loss. An improved version of the current Shashlik time resolution is also shown in Figure 8, based on a double-sided module readout and the use of Kuraray YS-2 and YS-4 WLS fibres for data taken at DESY and CERN, respectively. Future studies are being planned to investigate the rate dependence of the time resolution, the effects of PMT ageing, and the optimization of the signal-to-noise ratio.

The results obtained through the R&D work performed in WP3.2 have been included in the Framework TDR for the LHCb Upgrade II [4], submitted to the LHCC in December 2021.

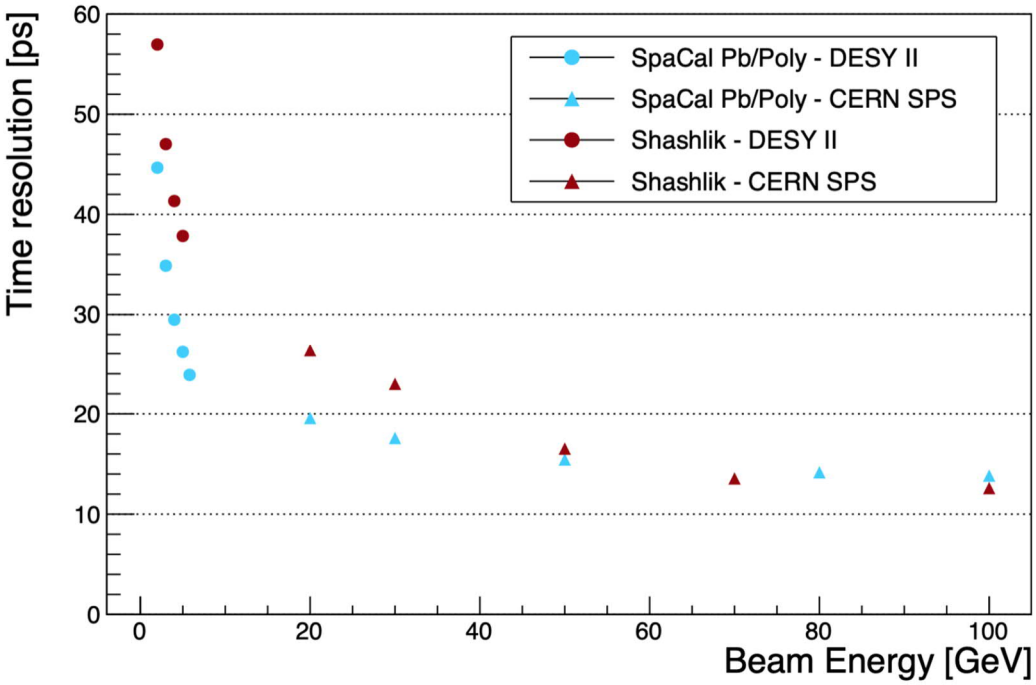

Figure 8: Time resolutions for SpaCal and Shashlik as measured in test beam.

4. Publications and contributions to conferences and workshops

Publications:

- [1] L. Martinazzoli, N. Kratochwil, S. Gundacker, E. Auffray, "Scintillation properties and timing performance of state-of-the-art Gd3Al2Ga3O12 single crystals", NIM A, 1000, 2021, 165231, https://doi.org/10.1016/j.nima.2021.165231
- [2] L. Martinazzoli, et al., "Compositional Engineering of Multicomponent Garnet Scintillators: Towards an Ultra-accelerated Scintillation Response", submitted for publication
- [3] R. Cala', et al., "Characterization of mixed $Bi_4(Ge_xSi_{1-x})_3O_{12}$ for crystal calorimetry at future colliders ", accepted for publication in NIM A
- [4] LHCb collaboration, "Framework TDR for the LHCb Upgrade II Opportunities in flavour physics, and beyond, in the HL-LHC era", December 2021, https://cds.cern.ch/record/2798645

Presentations:

- M. Salomoni on behalf of the LHCb ECAL Upgrade II R&D group, "The Upgrade II of the LHCb calorimeter", TIPP May 2021
- P. Roloff on behalf of the LHCb ECAL Upgrade II R&D group, "Scintillating sampling ECAL technology for the Upgrade II of LHCb", EPS-HEP July 2021.
- L. Martinazzoli on behalf of the LHCb ECAL Upgrade II R&D group, "Scintillating sampling technologies with precision timing capabilities for the Upgrade II electromagnetic calorimeter of LHCb", Workshop on Picosecond Timing Detectors for Physics September 2021.
- L. Martinazzoli on behalf of the LHCb & Crystal Clear SPACAL R&D group, "Prototyping and Testbeam Results of a Tungsten-Crystal Spaghetti Calorimeter", IEEE NSS & MIC October 2021.
- M. Pizzichemi on behalf of the ECAL Upgrade II R&D group, "Scintillating sampling ECAL technology for the Upgrade II of LHCb", VCI February 2022.
- L. Martinazzoli, "Scintillation Properties and Timing Performance of State-of-the-*art* $Gd_3Al_2Ga_3O_{12}$", LUMDETR 2021

- R. Cala', "Characterization of BGSO for crystal calorimetry of future colliders", LUMDETR 2021.
- R. Cala', "Characterization of BGSO for crystal calorimetry of future colliders", IEEE NSS/MIC conference 2021.

Posters:

- L. Martinazzoli on behalf of the LHCb ECAL Upgrade II R&D group, "*Development of Sampling Modules for the Upgrade II of the LHCb ECAL*", LHCC 2021.
- F. Betti on behalf of the LHCb ECAL Upgrade II R&D group, "Scintillating sampling ECAL technology for the Upgrade II of LHCb", The 30th International Symposium on Lepton Photon Interactions at High Energies, January 2022.

WP3.4 R&D on RICH detectors for future high-energy experiments

(Summary prepared by C. D'Ambrosio and F. Keizer)

1. Introduction

The EP R&D on RICH detectors focuses on: the development of an opto-electronics chain with O(100 ps) or better time resolution; the low-temperature and cryogenic cooling of SiPMs; lightweight composite mirrors and supports; and studies of novel Cherenkov radiators. In 2021, a prototype opto-electronics chain, based on SiPMs and MAPMTs coupled to the new FastIC ASIC and a TDC, was developed and tested at CERN's SPS. In addition to an important demonstration of the concepts and technologies for a future RICH detector with fast timing, this provided a strong foundation for further R&D including the implementation of cryogenic cooling. These activities were carried out by CERN and its closely-collaborating LHCb RICH institutes. A customisation of the FastIC ASIC, called the FastRICH ASIC, is foreseen and will include RICH specifications including an on-chip TDC in a radiation-tolerant design, which will be developed by the University of Barcelona and CERN EP-ESE, with input from the RICH group. A fellow is funded through EP R&D for this work package. The R&D into SiPMs and their integration in a small-scale detector demonstrator with cryogenic cooling has synergy with AIDAinnova task 8.4.

2. Main activities and achievements in 2021

2.1. Front-end electronics with fast timing

Owing to the prompt Cherenkov emission and focusing optics, the photons from a track arrive nearly simultaneously at the detector. This time information is critical to mitigate the effects of dark currents and pile-up in HL-LHC applications. Therefore, the 2021 R&D focus both at and outside CERN has been on developing and testing a prototype opto-electronic chain with SiPMs to provide fast-timing information. The next R&D phase will aim to lower the operating temperature of this chain in order to reduce the dark current further.

The prototype readout chain including the FastIC ASIC and TDC-in-FPGA is shown in Figure 1. The FastIC has a wide input bandwidth allowing the readout of various sensor types. In the future, the TDC functionality will be moved from the FPGA into a new radiation-tolerant version of the ASIC [1]. The analysis of the time resolution of the chain is ongoing, and further beam tests of the system are foreseen for 2022 along with a publication of the results. A test bench at CERN was developed for detailed time resolution studies using a picosecond pulsed laser.

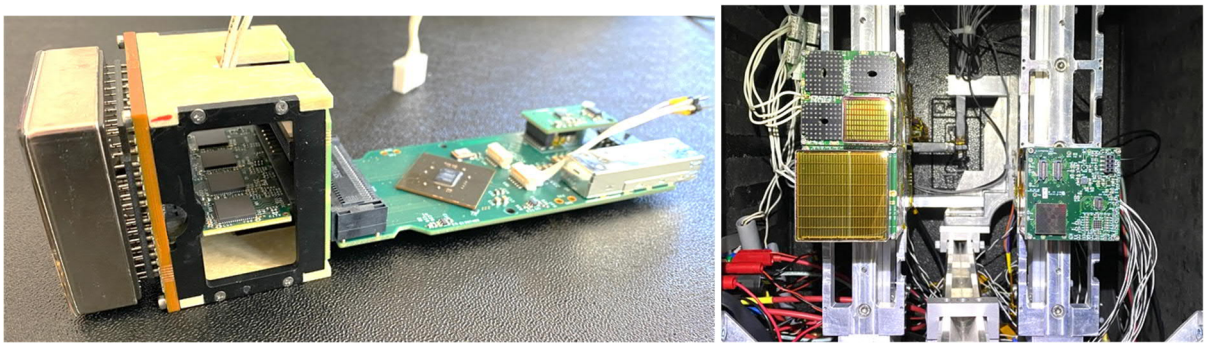

Figure 1. Prototype opto-electronic readout chain including the FastIC ASICs mounted on RICH front-end boards (left) and the readout coupled to SiPM arrays and MAPMTs at CERN's SPS beam tests.

2.2. Sensor characterisation and cryogenic cooling

A market survey of packaged SiPM arrays is ongoing with the aim of developing a small-scale RICH prototype with e.g. 1024 channels (similar to a photon detector module in the Run 3 LHCb RICH). Studies on the integration with readout electronics, in particular the signal coupling and capacitance, were started in 2021 with the readout chain described in Section 2.1 and will continue with special attention to time resolution [2]. We have met with cryogenic experts at CERN to start the discussion on integration of SiPM cooling to reduce the dark-count rate in RICH detector designs and intend to integrate some of these concepts into the small-scale prototype.

2.3. Novel radiator studies and test beams

The R&D into fast-timing readout and photon detectors provides a new perspective for studies of novel radiators, as signals from different radiators can be distinguished using time information (hence reducing potential combinatoric background) and SiPMs have a high photon-detection efficiency (allowing for a lower photon yield in the radiator). The Global Warming Potential (GWP) of the CO_2 radiator (GWP=1) used during the LHC pilot beam tests in the LHCb RICH is significantly lower than carbon fluoride counterparts (CF_4 , GWP=4880). Beam tests at the SPS demonstrated a good photon yield and transparency of novel hydrophobic aerogel [3]. The ongoing aerogel analysis and comparison to a Geant4 simulation will be published, together with our collaborators, in 2022.

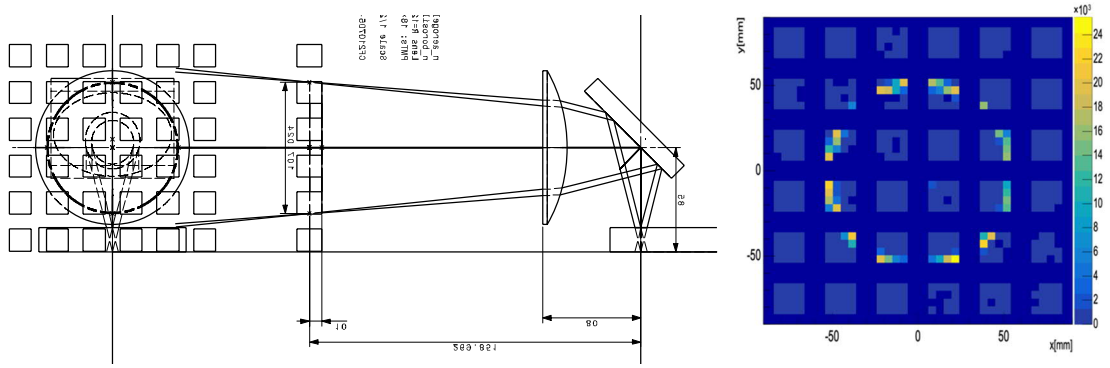

Figure 2. Technical drawing of test beam setup for aerogel studies in a focused arrangement using a mirror and lens (left). Measured data on the MAPMT array (right) matched the expected Cherenkov ring position.

2.4. Light-weight composite mirrors and supports

In the current LHCb RICH 1 detector, carbon-fibre-based spherical mirrors (with ~ 1% X_0) and support structure are already developed and produced by CMA (AZ, USA). R&D is needed to develop flat mirrors, to improve the quality and radiation length of the mirrors, to reduce cost and to follow new

developments such as Si-Carbide mirrors (up to 1.5 m and ~ 5 kg/m^2). A first flat carbon-fibre mirror prototype has been produced for RICH 1 and will be studied in the future.

3 Publications and contributions to conferences and workshops

Publications are in preparation for the aerogel measurements and SPS beam test campaign.

F. Keizer, "Novel photon timing techniques applied to the LHCb RICH upgrade programme", JINST, TIPP2021 proceedings (Poster presentation, also presented to the LHCC).

"Proposal for LHCb RICH detector enhancements during LHC Long Shutdown 3", CERN-LHCb-PUB-2021-014. (this is also Reference [1] in the above text).

References

[2] LHCb Collaboration, "Framework TDR for the LHCb Upgrade II – Opportunities in flavour physics, and beyond, in the HL-LHC era", CERN-LHCC-2021-012.

[3] M. Tabata et al, "Hydrophobic silica aerogel production at KEK", NIMA 668 (2012) 64-70, doi :10.1016/j.nima.2011.12.017.

WP3.5 R&D on SciFi detectors for future high-energy experiments

(Summary by S. Jakobsen)

A novel concept for scintillating plastic fibres has been investigated with Geant4 simulations. A new structure and wavelength shifting dyes are expected to lead to higher light output. Two fibre variants have been simulated. For this purpose, Geant4 had to be upgraded (released in v10.7) in order to allow for mixtures of wavelength shifters in the same volume. The simulations are now completed and have been documented in a confidential technical note. The simulation shows a gain in light output of up to 85%. The new fibre concept is also expected to be more radiation tolerant than the current generation.

Based on the promising results in simulation, a collaboration with the fibre producer Kuraray has been initiated. At this moment the producer is still trying to procure dyes with the desired properties. If successful, a prototype fibre will be fabricated and characterized at CERN.

WP4 Mechanics

1. Introduction

Work Package 4 (WP4) focuses on new solutions for mechanical supports and thermal management of future tracking detectors, on an ultralight detector's cryostat, and on maintainability of and access to particle detectors through a more automated mechanical and services connectivity.

The engineering effort on new solutions for mechanics is mainly focusing on near-future applications, like the ALICE Inner Tracking System 3 (ITS3) upgrade for RUN4 (section 2.1.1) and the IRIS tracker for RUN5 (2.1.2). In parallel new solutions for long term development on mechanics and cooling technologies are being investigated (sections 2.1.3 – 2.1.5). The research and development efforts on tracker mechanics and cooling are aligned with the AIDA-Innova programmme with which resources and industry support are being synchronised and shared.

WP4 is also evaluating the advantages and implications of a full carbon composite design for next-generation ultralight cryostats used in Detector Magnets and Liquid Argon (LAr) Calorimeters (section 2.2). Prototypes have been produced and tested to validate leak tightness across the wall of a carbon composite cryostat and carbon flanges sealed interfaces.

Concurrently, WP4 has also started a detailed analysis to identify the needs of future detectors for automated and robotic solutions for inspection, opening, access, and maintenance (section 2.3). Concrete, immediate needs have been identified in the current LHC detectors through a close exchange with the Technical Coordinators of the experiments, and some robotic solutions that could be applied for the remote inspection of the current detectors are being investigated.

The Working Group relies on young and motivated students (n. 2 on tracker mechanics and cooling, n.2 student on robotics) and fellows (n.2 on tracker mechanics and cooling, n.1 on carbon composite cryostats, n.1 on robotics) who have enthusiastically worked at the different development lines despite the adverse period.

2. Main activities and achievements in 2021

2.1 Low mass tracker mechanics and cooling

2.1.1 ITS3 (ALICE RUN4)

To minimise the material in the acceptance area of future trackers, a study to design a detector without an electrical substrate and without an active liquid cooling circuit was started [1]. Based on a close link between WP4 and the ALICE experiment, the study focuses on the ALICE ITS3. WP4 aims at developing the mechanics and cooling system for this detector with a design based on curved wafer-scale ultra-thin silicon sensors (down to 50-30 um) arranged in perfectly cylindrical layers, featuring an unprecedented low material budget of 0.05 $\%X_0$ for the three innermost layers. This represents an order of magnitude improvement compared to 0.3 $\%X_0$ for the present ITS three innermost layers.

Regarding the mechanics, in 2021, members of WP4 successfully assembled a first half detector prototype with dummy silicon sensors having a thickness of 40µm (Figure 1.a and 1.b). A procedure and a set of jigs have been developed to allow bending the large (280x94mm), fragile sensors and gluing the carbon foam (ALLCOMP HD, SD [2], carbon ERG Duocel@[3]). The latter, interleaved between the three layers, keeps the sensors bent.

Regarding the cooling, a forced airflow (4-8 m/s) between the layers should remove the heat that is generated by the sensors (5.1 W concentrated at the edge of the sensor and 3W distributed on the rest of the surface, Fig 1.c). The possibility to effectively remove the dissipated heat at each layer has been demonstrated by tests with breadboard models, and dummy layers, in a wind tunnel. Tests

showed that an air speed between 4 and 8 m/s maximise the heat removal and minimise sensor vibrations. In order to enhance cooling at the sensor edge, carbon foam radiators are being investigated. To characterise different carbon foam materials (Allcomp Standar Density, All Comp High density, ERG) tests and Computational Fluid Dynamics (CFD) simulations, are ongoing. Future work will investigate long-term stability performances, thermo-elastic behavior, and aeroelastic vibrational stability.

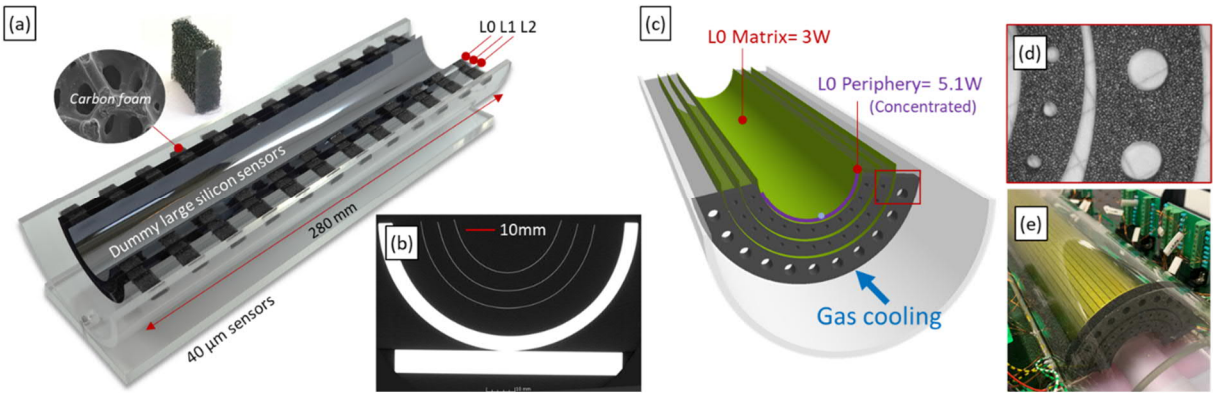

Figure 1 ALICE ITS3 prototypes: (a) half detector prototype with prime silicon sensors, (b) x-ray computed tomography of the three silicon half layers, (c) baseline design of the ITS3 prototypes with implemented half-ring radiators, (d) detail of the carbon foam radiators, (e) ITS3 prototype with implemented heaters and half ring cooling radiators.

2.1.2. IRIS (ALICE RUN 5)

In addition to the material budget minimisation requirement, positioning the first sensor layers as close as possible to the interaction point (IP) represents another major requirement for future generation vertex detectors. In view of the ALICE upgrade for LHC Run 5 [4], WP4 started working on a futuristic concept of a retractable vertex detector inserted inside the beampipe (see Figure 2). The tracker is mounted such that it can be retracted during LHC injection (minimum required aperture R_{min} = 16 mm) and placed close to the interaction point for data taking (R_{min} = 5 mm). A similar concept is followed by the LHCb VELO [5], which is not surrounded by other detectors. This is not true for the ALICE Vertex, which should cover large acceptances, including the mid-rapidity region. This requires a design of the IRIS and of the related moving and vacuum systems that minimise the amount of material in all directions. Since apertures, impedance, and vacuum stability for the vacuum chambers at the interaction points inside the LHC experiments are of extreme importance to the stable operation of the LHC, severe engineering challenges are imposed.

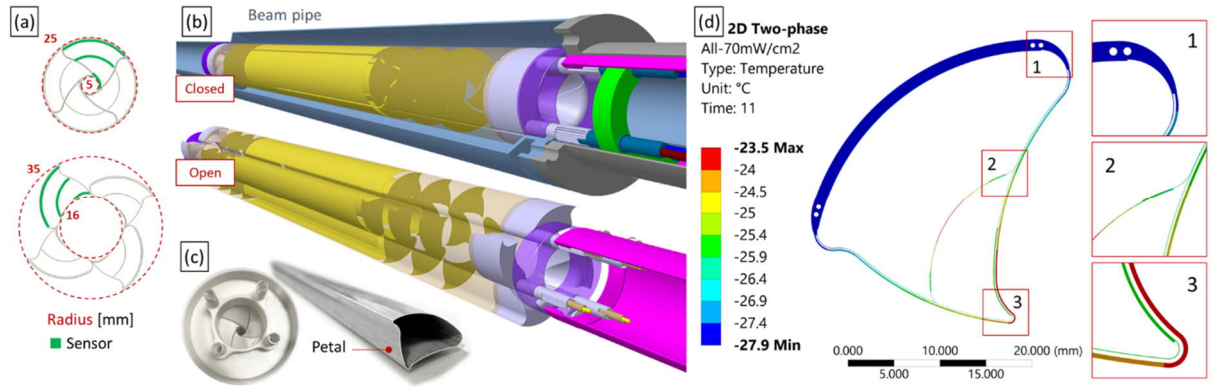

Figure 2 ALICE3 vertex detector: (a) A front view of the IRIS petals in the open and closed position is shown, the three sensors in each petal are highlighted in green. (b) The 3D CAD models show the in-vacuum layers housed inside the beam pipe and secondary vacuum. (c) First prototypes in aluminum and ACCURA25 were made for the petal walls and the IRIS rotary gear. (d) Preliminary 2D thermal analysis for the petal module.

The retractable tracker is constituted by four different modules (Figure 2.a), called Petals. Three layers of sensors are housed inside each petal in a secondary vacuum environment. The petals can simultaneously rotate and close, like in an iris optics diaphragm. In the close configuration, they leave a minimum passage of about 5 mm in radius for the beam, see Figure 2.a and 2.b. The petal walls (Figure 2.c), which separate the detector from the primary LHC vacuum, are the dominant contribution to the material budget and their thickness must be minimised. The wall of the petals oriented towards the beam acts as a radio-frequency (RF) foil, that controls the electromagnetic fields induced by the beam. Since this is equally relevant for the open and close positions, the petal geometries are designed to achieve an almost closed round bore when opened or closed, respectively (Figure 2.a). A further critical challenge is to develop the mechanics and vacuum equipment to preserve the possibility of access for maintenance.

An on-detector active cooling is required to cool the sensors (70 mW cm^{-2}) and to remove the heat generated in the petals' walls by the LHC beam (90 mW cm^{-2}). The attachment of a microchannel thin cold plate to the last layer inside the vacuum is under study. Preliminary thermal simulations, assuming the use of CO_2 evaporative cooling, indicate that such a design allows the operation of the vertex detector at −25 °C with a temperature spread across the silicon surface below 10 °C (Figure 2.d).

2.1.3. 3D printed microchannel substrate and connectivity (LEGO concept)

Silicon microchannel cooling substrates that can operate with single-phase and two-phase refrigerants represent a high-performance cooling solution adopted in recent years in Vertex detectors, like for the LHCb Velo and the NA62 GigaTracKer [6]. However, Si microchannel substrate dimensions are limited to the Si wafer-scale (up to 12 inch). Thus, the hydraulic interconnection between cooling substrates represents the challenge for implementing microchannels in large tracking detectors.

The rapid evolution of additive manufacturing (AM) opens the possibility to make AM microchannels substrates. AM technology allows producing complex cooling structures that can span over three-dimensional surfaces. Ceramics materials can also be 3D printed. Ceramics have always attracted the mechanics of the HEP experiments for their high radiation damage tolerance and thermoelastic compatibility with the silicon sensors. They can be used for applications where the operating temperature is below 0 °C.

WP4 is developing mini/microchannel substrates based on AM using either polymers (acrylic and epoxy-based photosensitive resins) or ceramics (Zirconia, Alumina, Silicon carbide, Aluminium nitride). The substrate design proposes a solution for the modules' hydraulics and mechanical interconnection (interlocking Modular microfluidic Cooling Substrate, i-MµCS), Figure 3 [7]. A plug-n-play in-plane hydraulic interconnection (Figure 3.a and b), based on micro O-ring to seal the two adjacent modules (Figure 3.c), is mechanically locked through a LEGO® like feature (Figure3.a and d). Polymers and ceramics (Zirconia and Alumina) prototypes were produced and extensively tested on a breadboard model scale.

Based on the first optimisation on polymer prototypes, the Interchangeability, i.e., the ability to select modules at random and fit them together within proper tolerances, guarantees the substrates' correct positioning and alignment within ±20 µm. The pull force needed to remove a substrate from its baseplate must ensure a proper mounting and dismounting capability that can be correlated to a minimum pull force of 1.5 N. At the same time, it must avoid sensors damage during assembly. The required pull force is also linked to the final substrate dimension. The pull forces were measured between 1.5 N and 7 N for polymer samples, depending on the number of contact points, i.e. engaged pins. The static friction coefficient also determines this force, and it depends on the materials of the baseplate and substrate. In this research phase, the study was not focused on the necessity to reach a specific range of force but, instead, on designing a customisable pin where its geometry can be tuned

to increase or decrease the stiffness of the mechanical interface. In this way, it is then possible to adapt the pull force according to the requirement of the final application. The hydraulic interconnected prototypes were tested up to 4 MPa with demineralised water as a refrigerant (Figure 3.e).

After the polymeric substrate characterisation, ceramic samples, in Alumina and Zirconia, were produced with two different AM technologies, the NanoParticle Jetting technology (NPJ, Xjet company [8]) and the Lithography-based Ceramic Manufacturing (LCM, Lithoz company [9]). X-ray computed tomography and 3D scan were used to inspect internal defects, and measure the dimensional accuracy of the features, surface flatness, and roughness. Permeability tests and roughness measurements were performed for the embedded channels with diameters down to 0.5 mm.

The above tests show that is possible to produce ceramic cooling substrates with AM technology without relevant issues. Indeed, no relevant internal defect of the produced parts was noted; all samples were printed with a relative density greater than 98%; the feature accuracy was less than ±50 µm; the surface finishing was N8-N9 while R_a of the inner channel was less than 20 µm. A similar qualification of the hydraulic and mechanics interconnection for ceramics prototypes was followed. Ceramic prototypes can be positioned within ±100µm of accuracy; the pull-force tuned from 1 to 20 N, and they withstand pressures up to 6 MPa. The path of applying ceramic substrates in a future detector application is still at the beginning. Synergies with the AIDAInnova program have started to characterise the ceramic 3D printed technologies fully.

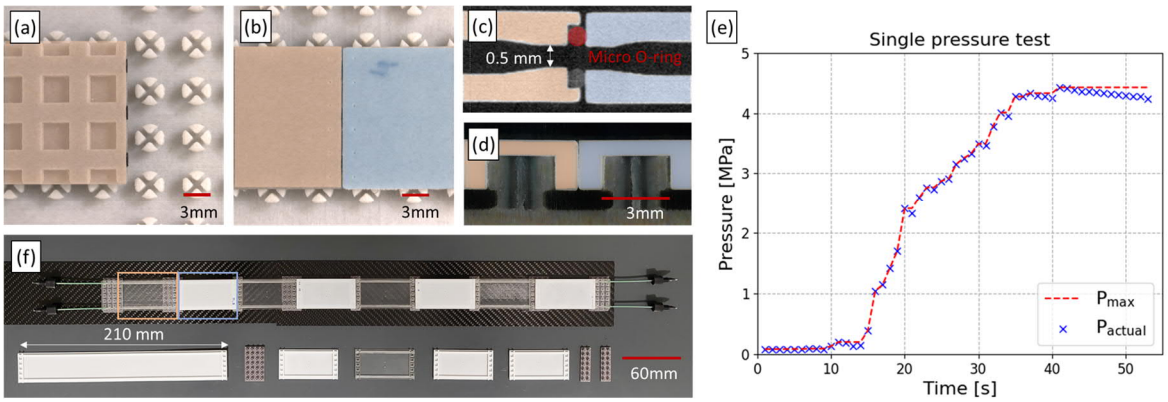

Figure 3 Interlocking modular microfluidic solution: (a-d) Details of the breadboard model, (e) pressure test and (f) assembly of i-MµCS modules integrated on a possible detector layout.

Alumina i-MµCS with dimensions of the hybrid integrated circuit of ALICE ITS2 (210 x 30 mm^2) were produced to qualify the concept on the detector scale (Error! Reference source not found.). Thermal tests with demineralised water as a refrigerant are now ongoing. Interconnection variants have been designed, analysed, and breadboard models developed and tested. Variants of the hydraulic interconnection demonstrate withstand pressure up to 20 MPa.

2.1.4. Carbon cold plate for CO2 two-phase cooling solutions

An alternative solution to microchannel substrates, in state-of-the-art trackers, are lightweight composite structures with an embedded network of metallic or plastic pipes containing the cooling fluid.

Investigation in WP4 have started from the cold plate design originally developed for the ALICE ITS upgrade, based on a low-mass carbon substrate with embedded small diameter pipes. Compared to the initial application of ultra-thin Kapton pipes subjected to low-pressure single-phase and two-phase flows of water and C_4F_{10}, the main challenge was to adapt the existing technology to the high saturation pressures of evaporating carbon dioxide, for two-phase cooling solutions. The opposing test conditions of thin-walled tubes and high working pressures asked for a reviewed research approach, where the

CERN CO_2 test facility for mini and micro-channels [10-11] is employed for the required two-phase flow tests (Figure 4.a and 4.b). As a first proof-of-concept, an existing ALICE ITS inner barrel stave sample was pressure tested and installed into the vacuum vessel of the test set-up and subjected to flow boiling tests where the heat load was supplied by means of a thin-film Kapton heater. To carry out a direct comparison the test parameters (mass flux, heat flux, inlet vapour quality) were adapted to the values given in the study on C_4F_{10} [12] and were limited to a saturation temperature of -20°C (~20 bar) due to the reduced hoop strength of the thin-walled tubes. Circulation of CO_2 was possible, and a first demonstration of the effectiveness of the cold plate was documented with infrared images. The ΔT between CO_2 and sensor of the order of 8-10 ºC, for a mass flux range 300-1000 kg m^{-2} s^{-1}, is very similar to the one measured for C_4F_{10} .

Additionally, CO_2 compatibility and permeation tests were carried out with polyimide samples. Both tests point towards a negligible long-term effect. In the next step, in order to extend the test parameters to higher saturation temperatures (and pressures), thus to the most favourable thermo-physical regime of evaporative CO_2, new thick-walled polyimide tube specimen had to be procured and were implemented into a revised cold plate design, while equivalent cold plates will be produced with stainless steel tubes as reference. Production of cold plates will be supported by an industrial partner of the AIDAInnova programme, with whom the WP4 is starting sharing the development and chracterisation.

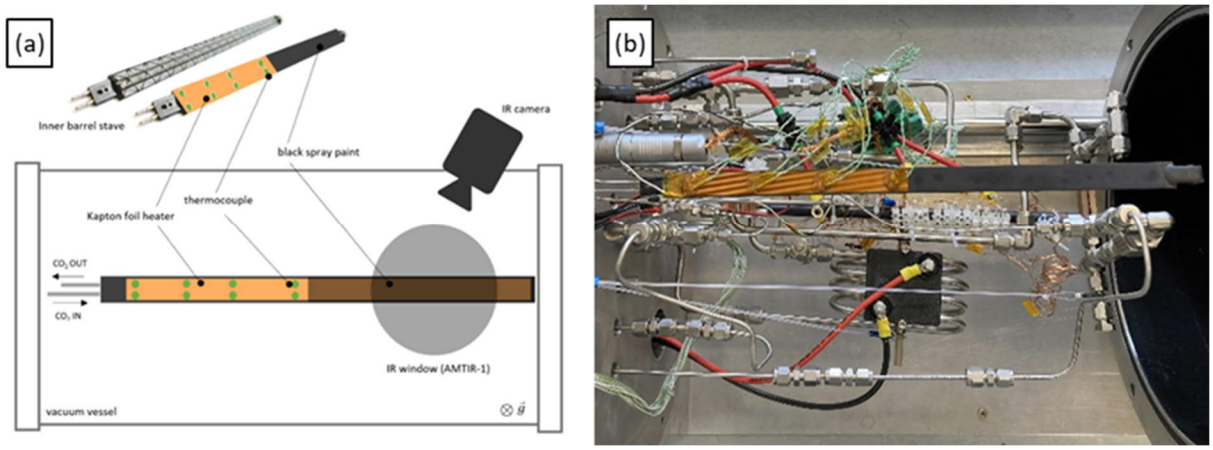

Figure 4 CERN CO_2 test facility for mini- and micro-channels with ITS inner barrel stave sample inside the vacuum vessel: (a) schematic concept and (b) actual installation. For an initial hybrid approach, the surface of the heater that simulates the glued chips was monitored by means of thermocouples glued along the first half and a thermal camera pointing to the second half of the stave through an infrared window in the set-up's vacuum vessel.

2.1.5. Carbon cold plates with engraved micro-vascular networks

The performance targets of future HEP experiments call for even lighter and more efficient technologies, where the challenge is into removing completely the embedded pipes in the substrate. The use of sacrificial materials to create micro-vascular networks in the composite laminates represents a very appealing solution to engrave the cooling circuit in the support carbon structure.

The VaSC (Vaporization of Sacrificial Components) process has been tested to manufacture carbon composite plates with longitudinal channels. Different modified poly(lactic) acid (PLA) preforms have been co-cured inside epoxy-carbon composite laminates having laminae of T800/ER450 and orientation $[0,90,0]_S$. Next, a post-cure step at 200°C in a vacuum oven has been used to vaporise the PLA pre-forms [13], yielding embedded channels with different cross-section geometries and dimensions (Figure 5.a, 5.b).

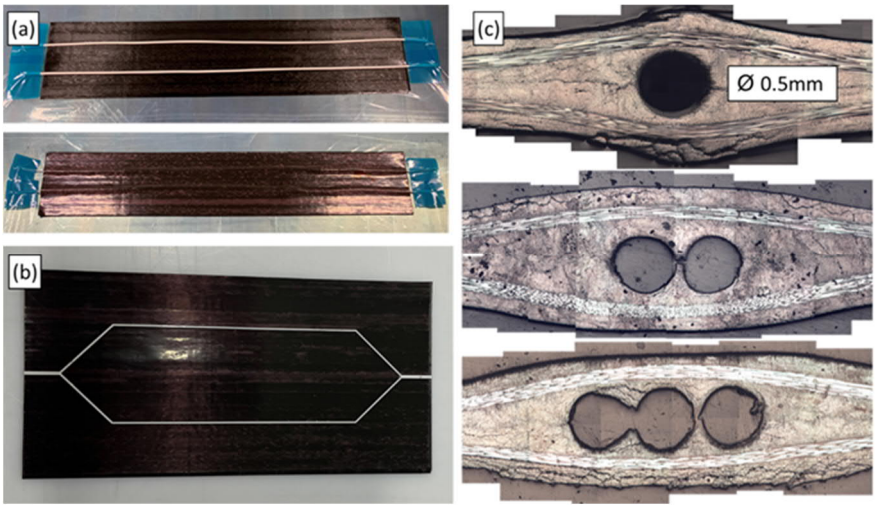

Figure 5 Carbon cold plate with engraved micro-vascular networks: (a) Production of the first asymmetric sample, (b) channel network produce with water jet cutting, (c) microscope cross section view of three samples made with an assembly of PLA fibers,.

X-ray computed tomography and microscope analysis revealed clean and regular channels in test samples up to 600 mm long (Figure 5.c). As can be seen from Figure 5.c, the quality of the single channel decrease when more channels are present in the structure.

Destructive tests have been carried out to determine the burst pressure of the plates as a function of the cross-section of the channels. Burst pressures of 3 and 10 MPa were obtained for circular channels with diameters of 1.75 mm and 0.5 mm respectively, embedded in symmetric plates (T800/ER450, $[0,90,0]_S$). The deformation of the composite plates during the test was monitored using Digital Image Correlation (DIC).

The current results demonstrate that the VaSC process can be used to create micro-vascular networks in the composite laminates.

Future work will study how to improve the quality of the channels and produce a wider range of cross sections. Furthermore, it will use the test results to validate a finite element model under development. The numerical model will provide a tool to design an optimised structure with embedded channel networks. Numerical studies have been performed to simulate the fracture of the channels with a finite element model which relies on cohesive elements. Experimental delamination results obtained with mode I double cantilever beam (DCB) test specimens have been used to determine the input parameters for the fracture numerical model.

2.2 Ultra-light Cryostat

This project evaluates the use of carbon composite materials to design cryostats for Liquid Argon Calorimeters and/or Superconductive Magnets and if these cryostats are thinner than metal ones. The goal is to reduce the material budget to enhance physics performance of future detectors. After a literature study of R&D activities in the aerospace industry [14,15], a few key technological solutions tailored to CERN detectors requirements were identified and prototyping was launched for validation.

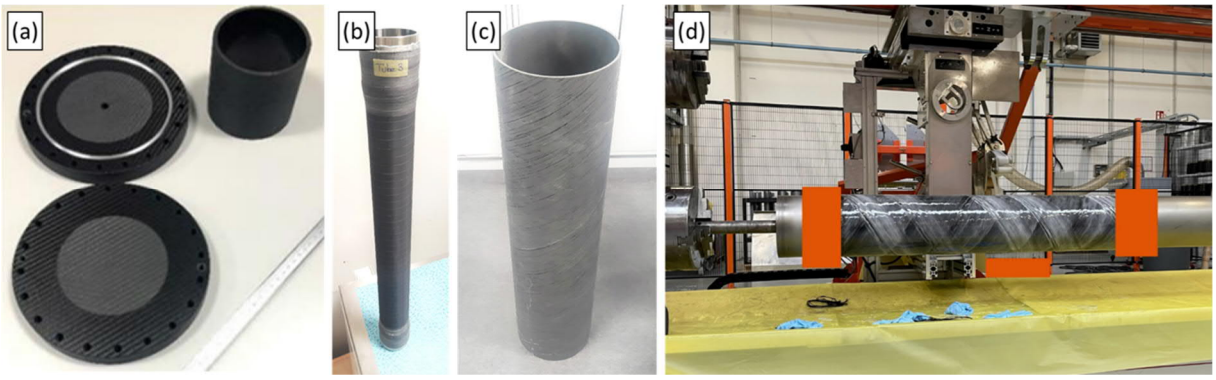

Figure 6: Prototypes for ultra-light cryostat: (a) Prototype 1 and 2, thin-wall shell and flanges by hand layup. (b) Prototype 3, pipe with metallic end-fittings by filament winding. (c) Prototype 4, thin-wall shell by filament winding (d) and its manufacturing process at Connova facilities.

Four prototypes were produced (Figure 6.a, 6.b, 6.c, 6.d) to address the main design features such as wall leak-tightness, carbon-carbon sealed connection, carbon/metal transitions, filament winding production process, toughened resin for cryogenic temperatures, Out of Autoclave (OoA) curing. Below short descriptions of the prototypes and of the characterisation tests performed on each of them.

Prototype 1 (Figure 6.a) aims to demonstrate the possibility to manufacture a carbon cryostat wall that, without any metallic liner, can provide leak tightness at 87K. The prototype is a carbon tube (100 mm diameter x 100 mm length) with 5mm wall thickness, laminated with CTD-133/IM7 prepreg, a special carbon composite material developed for aerospace applications [16]. This prototype is built with a hybrid laminate combination of thick carbon plies (140 g/m2) (which can be placed relatively quickly) and thin plies (70 g/m2) to create a microcrack-resistant laminate, that helps to prevent liquid argon permeation. Leak tightness at nominal operative conditions (T=87K, P=3.5bar) was verified through a test campaign in a collaboration between WP4, CERN Cryolab & Instrumentation section and WP3 colleagues. The test results (Figure 7.a) show a He leak-tightness of the tube wall of 10^{-9} mbar.l/sec at 108 K (limited by the test set-up, shown in Figure 7.b) and 3.5 bars. Computed tomography driven by EN-MME-MM section has confirmed the absence of microcracks and its propagation due to the cooling down process (Figure 7.c 7.d)

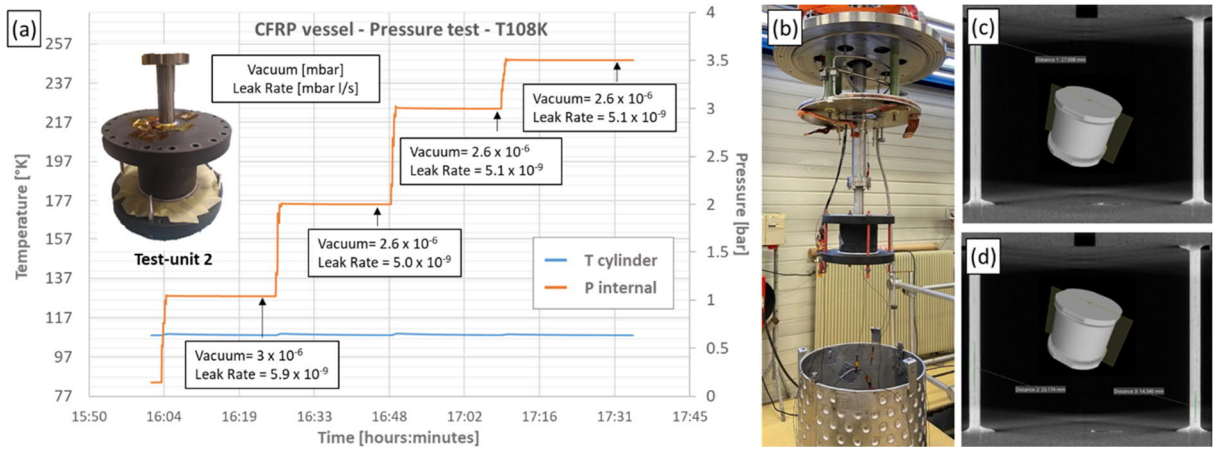

Figure 7 He-leak test: Results on prototype 1 (a). Experimental set-up (b). X-ray computed tomography before the cooling down process (c) and after the cooling down process (d).

Prototype 2 (Figure 6.a) is built to validate the sealing between two full carbon flanges. Matching carbon surfaces and sealing housing were machined to the required finishing accuracy (Ra 1.6 to 3.2), a Helicoflex metallic seal is used at the interface. Bolts connecting the two flanges are equipped with

a Belleville washers stuck-up to compensate for differential thermal expansion between carbon flanges and metallic bolts. Tests results validate the design up to a He leak tightness of 10^{-9}mbar.l/sec at 115 K and 3.5 bars, according to requirements.

Prototype 3 consists of thinner (down to 0.8 mm wall) carbon composite pipes (Figure 6.b), with embedded stainless steel end-fittings. The carbon/metal transition represents an alternative option for the design of metallic feedthroughs allocating the input/output lines of the carbon cryostat. To ensure the joint tightness, polymeric fibers wound in the radial direction around the flange diameter help to compensate for different thermal contraction of metallic and carbon composite parts. Samples were manufactured with CTD-7.1/T800H and LY556/ T800H, and tested to be He leak tight (down to 10^{-9} mbar l/sec) at room temperature with the help of CERN Cryolab. This investigation also poses a first step in the development of a carbon beampipe as an alternative to the standard beryllium design.

Prototype 4 (Figure 6.c) is a larger scale prototype that aims to identify the manufacturing process that will best suits CERN cryostat requirements. Wet filament winding for the fiber placement process and Out of Autoclave curing has been selected as an alternative to the Robotic Automated Fiber Placement (RAFP) technology [12,13]. A monolithic cylindrical shell of 1 m length, 0.3 m diameter and 5 mm thickness has been produced in close partnership with Connova [17] using aerospace resin CTD-7.1 (CTD-133 variant for filament winding), T800H fiber and $[-55/55]_s$ layup. Engineering assessments have been carried out to tune the standard process to work with CTD toughened epoxy resin and minimise final void content (vacuum evacuation of resin bath, plee-ply as final layer, non-crossing fiber placement, among other measurements).

The next steps foresees the manufacturing of another prototype (Prototype 5) with the same dimensions of Prototype 4 but with a different resin system, Araldite LY556, also used in aerospace at cryogenic temperatures. Both, CTD-7.1 (prototype 4) and Araldite LY556 (prototype 5) resins will be tested to operative environment levels including radiation resistance to load expected in FCChh and FCCee.

Final goal of the project investigation will be the development and construction of a large -1m in diameter- full carbon demonstrator, based on:

- High modulus carbon fiber to reach high mechanical properties and address buckling behaviour.
- Toughened epoxy resin (microcrack resistant) suitable for filament winding, to ensure leak-tightness under working conditions.
- Non crossing wound laminate: each ply is wound by the robotic arm without intersection to minimise void content. This will highly contribute to both, avoiding microcrack appearance at cryogenic temperature and improving the mechanical properties of the final structure.

2.3 Robotics

In 2021, the activities in WP4 on robotics refined the studies performed in the previous year [18,19] and particularly focused on the characterisation of the environment in current and future particle detectors [20], where the main challenges to using robots and automated systems are high radiation levels and the presence of magnetic fields.

According to the data available for future detectors [21-24], the highest requirements for robotics in terms of magnetic field to withstand are imposed in the FCC-hh, which in its conceptual design does not have a return yoke. According to simulation results [21], in the FCC-hh cavern, the magnetic field in might reach values as high as 0.4 T (outside the detector). This is an issue for most of the commercial robots and automatic systems since they are actuated by electromagnetic motors, which are affected by magnetic fields. The effects of high external magnetic fields on those motors are twofold:

1) The external magnetic field interferes with the magnetic fields that the motors generate internally to work, compromising its functionality.
2) The external magnetic field exerts a dynamic action (torques and forces) on the ferromagnetic component of the motors. This action influences the motion of the robot/automated system.

In literature there is little to no information about the behaviour of electromagnetic motors in high external magnetic fields, thus, a campaign to characterise such a behaviour was started.

Different electric motors were positioned inside a tuneable (up to 0.5 T), uniform magnetic field. The motors, unloaded, were fed with a fixed voltage, and the revolution per minute of the motors (RPM) was measured as a function of the external magnetic field magnitude. For the measurements, a laser RPM meter was used since this is not influenced by the magnetic field. Some of the considered motors had also internal Hall probes to measure their RPM. In the motors where the Hall probes were available, their measurements were compared with the laser RPM measurement. Also, the feeding current that was demanded by the motors was measured as a function of the external magnetic field.

In Figure 8, the data that were acquired from one of the tested motors are reported. Figure 8.a shows the feeding current and the RPM of the motor as a function of the external magnetic field when the motor is fed with 12 V tension, Figure 8.b shows the same data when the motor is fed with 24 V tension. In both cases, the RPM curve is approximately constant up to a certain external magnetic field threshold value (about 120 mT for the motor fed at 12 V and about 220 mT for the motor fed at 24 V). For higher values of the external magnetic field, the RPM decreases at the increase of the disturbing magnetic field. Finally, for a value of 150 mT for the motor fed at 12 V and 250 mT for the motor fed at 24 V, the RPM goes to zero, i.e., the motor stops turning. Interestingly, there is good agreement between the RPM measurements performed with the laser RPM meter and the Hall probes.

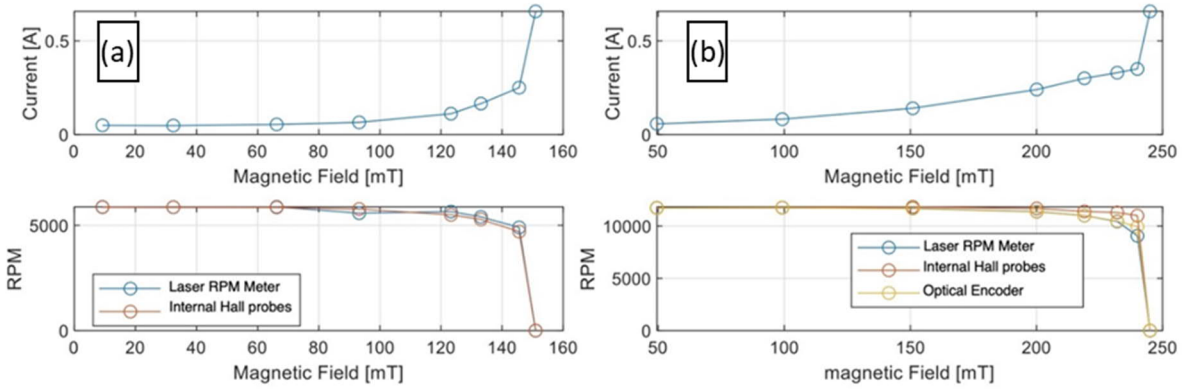

Figure 8 Data collection for Maxon motor EC-MAX 283840. Top, motor feeding current as a function of the external magnetic field. Bottom, the motor's revolution per minute (RPM) without load. (a) Feeding voltage 12 V (b) Feeding Voltage 24 V. For this test RPM data were additionally acquired using an optical encoder mounted on the motor.

Looking at the feeding current, it steadily increases with the external magnetic field. One can notice an abrupt increase of the feeding current at the value of the external magnetic field for which the RPM goes to zero. This can be explained considering that the external magnetic field exerts a disturbing torque on the rotor (a permanent magnet in the case of a brushless motor as the one analysed in this work) that acts to align the rotor steadily with the external magnetic field. To balance the disturbing torque, the motor must generate more intense internal magnetic fields, thus absorbing more current. For values of the external magnetic field above the threshold level, the internally generated magnetic field cannot completely compensate the external disturbance torque and the RPM starts to decrease, while the motor feeding current keeps increasing. When the external magnetic field reaches a level so high that it becomes the dominant field inside the motor, the rotor aligns with it and stops rotating.

The motor electronics, registering no motion of the motor, tries to generate stronger internal fields absorbing more current, eventually reaching the maximum current allowed in the motor. At this point, the control electronics triggers an error cutting the power line. If the motor has more power available, i.e. is fed with higher voltage, it can generate stronger internal magnetic fields, thus, increasing the threshold level. Other results not reported here show that brushed motors may have different behaviours in magnetic fields.

This study shows that electric motors can work correctly in a high magnetic field below a threshold level and that the value of the threshold magnetic field is a function of the power available to the motor, i.e. motors fed with more power could resist higher magnetic disturbances.

Regarding the forces and torques that an external magnetic field generates on magnetic motors, a mathematical model to predict those quantities was developed in collaboration with Scuola di Ingegneria Aerospaziale (SIA) of Università di Roma la Sapienza [25]. The model will be soon benchmarked against experimental data. Some preliminary results are shown in Figure 9.

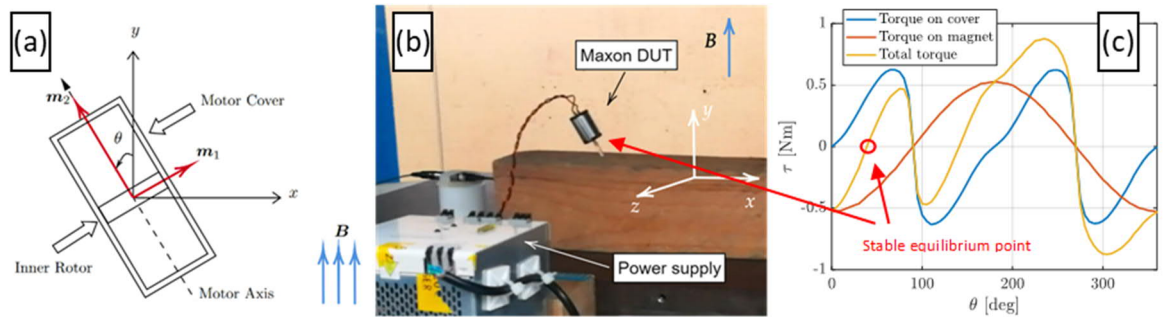

Figure 9 External magnetic field induced forces and torques: (a) Magnetic Motor Model. The electromagnetic motor modelled with two magnetic dipole moments, m_1 and m_2, perpendicular one with each other. The former represents the contribution of the motor external cover, the latter the contribution of the motor internal magnets. (b) Test of a real motor inside a uniform magnetic field, observe that the motor, indicated as DUT, is not laying on the ground because of the magnetic field torque. (c) The torque acting on the motor z axis computed with the developed model, preliminary results. The model predicts a stable equilibrium point for theta of around 40 degrees that seems to agree with the experimentation observations.

Furthermore, as another point of collaboration with SIA, a study for the development of a system of flying robots for the continuous mapping of the experimental caverns of current and future detectors has been developed. The research on the point is still ongoing, however, a master thesis is being published summarising the obtained results [26].

Some small low-cost quadruped robots, PETOI bittle [27], have been bought and tested in the magnetic field environment with encouraging results (the motors behaved as expected for magnetic fields up to 0.45 T). On those robots, a system that should guarantee communication also in very confined spaces is being tested. Furthermore, a radiation testing campaign for the robots is being organised in the CERN facilities.

WP4 is also in contact with companies producing bigger size quadruped robots (as for instance SPOT from Boston Dynamics [28] and ANYmal from ANYbotics [29]), investigating the possibility to test, in collaboration with the companies, the resistance of those robots against radiations.

Future work will investigate the applications of an indoor positioning system in the detector cavern to better implement the autonomous motion of robotic platforms (some preliminary activities are already studying the use of optic systems for this purpose). Another planned future activity is the design, implementation and test of control algorithms for UFVs and quadruped robots that take into account the magnetic disturbance forces and torques in the detector cavern. In parallel with this last

activity, web interfaces to communicate and control the robots using the CERN wireless networks will be developed. Finally, an irradiations campaign on the robots available at CERN will be organised.

3. Publications and contributions to conferences and workshops

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WP5 IC Technologies

1. Introduction

Microelectronics is widely recognised as one of the key enabling technologies for present day and future High Energy Physics experiments. At present most ASIC developments for the LHC upgrades are based on the 65nm node (with 130nm being used in less demanding applications). One of the aims of Work Package 5 is to provide the HEP community with a solid infrastructure in state-of-the art CMOS technologies and design methodologies for the development of complex mixed-mode ASICs for future applications. Another component of the work package is to develop novel approaches for DC/DC conversion allowing efficient transfer of power to the components in the heart of the detectors. To disseminate technical information to the HEP community as well as to help identify synergies and establish collbarations with external institutes quarterly technology forum session have been organized with participants from CERN and collaborating institutes [1-4]. At present WP 5 has 4 active components and there are 4 Fellows, 2 Technical students and 3 trainees currently being employed.

2. Main activities and achievements in 2021

2.1 IC Technologies - Technology evaluation

In 2021, one of the main activities of the Work Package 5 has been the performance evaluation and radiation tolerance characterization of the 28 nm bulk CMOS technology. The radiation studies focus on Total Ionizing Dose (TID) degradation as well as on Single Event Effects (SEE) on CMOS devices and circuits. The objectives are to provide design guidelines, a selection of design libraries, and the main IP blocks to enable the design of large, complex and radiation tolerant ASICs in this advanced node. The technology evaluation team dedicated the first part of the year to the design of a chip to study single transistors, the so-called TID28 chip, while during the second part of the year, they focused on the development of a chipset, namely EXP28, to study basic circuitry and macros.

2.1.1. The TID28 test chip

The TID28 chip was designed to study the effects of ionizing radiation on single transistors in TSMC 28nm HPC+ technology. This is the first chip designed on this technology for this objective. The chip was designed leveraging the experience developed during the study of 130nm and 65nm technologies, as well as the results obtained in a previous chip in TSMC 28nm HPC technology. The chip consists of eight independent structures, each facilitating the study of the TID response of specific parameters such as: dependence of the response to transistor size, increase in source-drain leakage current, influence of the applied bias voltage, influence of the transistor's threshold voltage, increase in transistor-to-transistor variability, increase in gate-leakage-current, effect of TID on segmented devices, response of sub-minimum size devices, increase in leakage current between adjacent MOSFETs, TID-response of I/O transistors and effect of TID on ESD protection circuitry. The device sizes were chosen to be comparable with those typically used in digital applications to provide more representative results of the degradation of a complex real-life ASIC. Error! Reference source not found. depicts the sizes of core transistors included in the chip. Three areas are identified: the red area indicates devices that are typically more sensitive to radiation; the green area identifies devices that are more robust to TID; the yellow area includes devices with sizes commonly used in digital applications.

The chip has been tested and all structures are working. Initial irradiations show that the radiation response of HPC+ technology is very similar to that measured in HPC, the latter having been extensively studied in recent years. Error! Reference source not found. shows the percentage degradation of the maximum drain current I_ON at increasing levels of TID, for pMOS transistors of different sizes in HPC

and HPC+. The radiation response is very similar in all devices. The same similarity is measured in nMOS devices. If the measurements continue to confirm the similarity between HPC and HPC+, the results observed in HPC can be used to support those obtained in the new chip. This chip will certainly be critical to understanding the possibilities offered by this technology in terms of radiation resistance, laying the foundation for the design of all future ASICs in TSMC 28nm HPC+ technology. The scope of our present studies is to evaluate the radiation resistance up to a TID of 1Grad. It is expected that these studies will strengthen our understanding of the radiation effects on this technology node and pave the way for possible eventual applications in the future FCC -hh accelerator attaining radiation levels of 30Grad in the inner tracker regions of experiments and for a total integrated luminosity of 30 ab^{-1}.

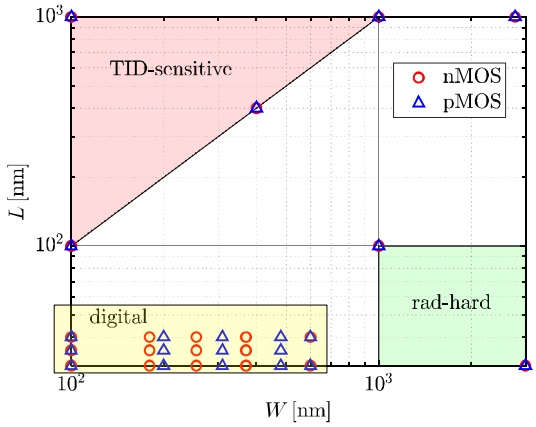

Figure 1. Sensitivity of devices to TID

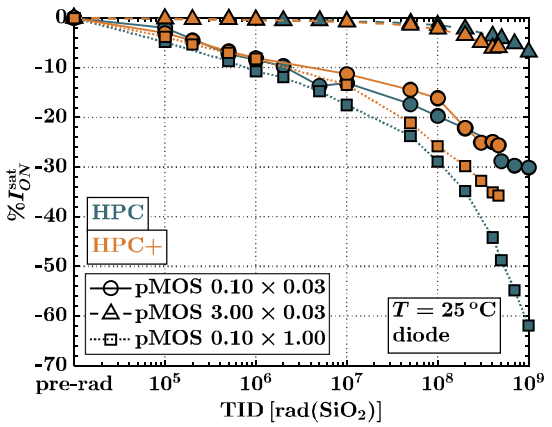

Figure 2. Saturation current degradation as a function of TID

2.1.2 The EXP28 chipset

The EXP28 is a family of chips designed to facilitate the SEE and TID studies on the 28 nm technology. These test chips incorporate a number of components such as foundry standard cell libraries, SRAM memories, single-ended and differential Input/Output pads and a number of IP blocks for characterization. These components are the enablers of more complex designs. The family of chips consists of the three chips described in the next paragraphs.

The EXP28_TID chip is dedicated for TID studies. It includes various types of circuitry such as a ring-oscillator (RO) for standard cell library degradation evaluation and a dedicated Built-In-Self-Test (BIST) circuit for testing the foundry SRAM block generated by the foundry memory compiler.

The EXP28_TID-RO circuitry allows the study of more complex digital structures with continuously switching activity. Measuring the oscillation frequency of the ROs will allow the evaluation of the impact of TID on the operation of MOS transistors. The frequency can be measured directly, thanks to pads connected to the output of the ROs, or via an internal counter. The value of the counter can be retrieved via an I2C interface.

The TSMC 28nm HPC+ technology offers several digital standard cell libraries, including transistors of different threshold voltages (ULVT, LVT SVT, HVT, UHVT and EHVT), different channel lengths (30 nm, 35 nm and 40 nm) and different track heights (7T, 9T, 12T), corresponding to different channel widths. Many of the libraries are power-gated, meaning that it is possible to selectively power on/off one or more libraries. The power gating technique allows the contribution to power dissipation of each RO to be separated, without requiring 2 pads for each device to power them independently. For each of the 23 libraries, 16 ROs consisting of a different chain of cells were designed: clock buffers, inverters and several combinatorial logic cells are included as well as sequential cells like d-flip flops and latches. The

large number of available ROs will enable detailed analysis of the response of the technology to TID, guiding the design of future ASICs in TSMC 28 nm HPC+.

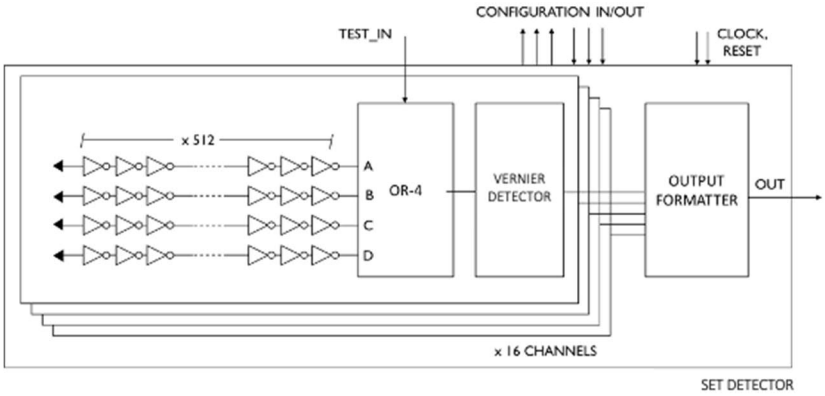

Figure 3. Structures for Single Event Transient (SET) studies on the EXP28_SEE test chip

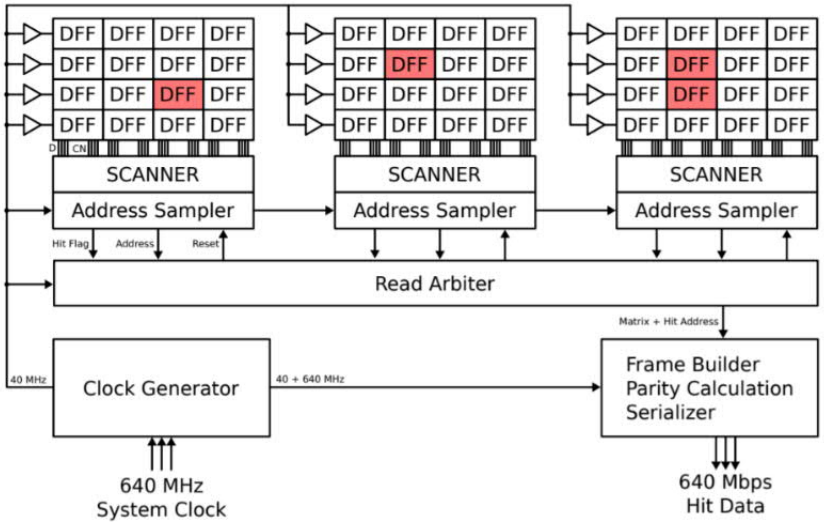

Figure 4. Structures for Single Event Upset (SEU) studies on the EXP28_SEE test chip

EXP28_TID-BIST circuitry utilizes foundry SRAM blocks with integrated Built-In-Self-Test (BIS) circuitry to implement a fully integrated methodology for at-speed radiation testing of memories enabling studies that are not feasible with the conventional parallel bus I/O approach. The electronics for testing are embedded on-chip and run at higher speed than the memory under test. The test chip includes four different types of SRAMs with different cell-type, density, and access type: single port, single port Ultra High Density (UHD), dual port and dual port UHD. The BIST for these memories is reusable and exploits different algorithms: for single port SRAMs exploits a March C- algorithm while dual port SRAMs requires more complicate algorithm (1PF1s, 2PF2s, 2PF1s, 2PF2s, 2PF3s ref.) to test independently and simultaneously the two ports. This testing methodology allows to monitor the degradation of the memory access time during the irradiation, in addition dedicated power supplies for each memory type allow to monitor leakage current independently.

The EXP28_SEE test chip, is dedicated to SEE studies. It includes test structures for Single Event Transient studies based on Vernier Delay Line, for Single Event Upset studies on sequential elements based on matrices of Flip-Flops and for Single Event Effect on memories from the foundry compiler.

Single Event Transients (SETs) are a major concern for HEP application, particularly when hardened flip flops are used to reduce the sensitivity of sequential logic. Characterizing SETs is complex as both the cross-section and the pulse width must be measured. In this test chip a SET measurement circuit based on a Vernier delay line is implemented (Figure 3). The architecture is based on the references [1] and [2] and is divided in target circuit, vernier detector and output formatter as shown in the figure. The detector contains 16 channels and therefore the output formatter acts also as arbiter and serializer. Each channel contains a target circuit made of four chains of minimum size inverters of 512 elements. The elements from the 16 channels are interleaved to detect multiple SET: all inverter chains "A" are one next to the other, then the "B" and so on. The total area covered with the target circuit is approx. 400 x 80 um2.

Single Event Upset (SEU) test structures (Figure 4) are intended to evaluate single and multi-bit upsets in sequential elements (D-Flip Flop). The test structure is derived from a test chip designed to test multi-bit upsets in 65nm [3]. The block scheme is reported in Figure 3. It presents 7 matrices of 4096, non-triplicated, DFF continuously clocked, with D tied to Q, in several flavors: with and without output buffer, different driving strength, different threshold flavor and with spacing. A rad-hard data processing and readout logic encode and transmit the information about the elements hit by SEUs. From the user point of view, only one input clock line (up to 640MHz) is needed, and data is transmitted serially through one single output line at the same clock speed (up to 640MHz). The test structure output contains the location of single or multi-bit upset. The readout rate is one packet every 40 MHz.

The so-called SRAM-SEU test structure is intended to test under SEUs SRAMs generated with the foundry compilers. The block is designed to allow the user to perform read and write memory operations and evaluate the SRAM response during irradiation. As in the TID chip, different type of SRAMs are included (single/dual port, normal and ultra-high density). The different types of SRAMs are repeated to cover a total active area of 0.76mm2. Each SRAM, as well as the functional logic and serializers/deserializers, is provided its own power domain to study separately the effects under SEUs. Serial input and output lines allow to control all the SRAM pins. Input bitstream (64 bits) contains control (read/write, address, enable) and data bits for the different SRAMs. Serializers are used in output to serialize data read from SRAMs. Apart from the following constraints, all SRAM operations are possible through the serial lines, providing full control on the memory blocks and allowing to choose its own test routine.

The EXP28_ANA test chip is dedicated to Analog IP block development and includes a bandgap, a temperature sensor and a DAC described in the IP block section. In addition, it contains a test structure dedicated to Single Event Latch-up (SEL) studies as well as a probing array as the TID28_CHIP for resistor and HV transistor TID studies.

These three ASICs were submitted for prototyping on a Multi-Project-Wafer (MPW) run in December 2021. Characterization and performance evaluation is expected to take place during 2022.

2.2 Analog IP blocks

The objective of this activity is to build know-how on the 28nm CMOS technology and on the design tools, by designing and characterizing circuit IP blocks that will be used on complex ASICs for the HEP community. A core objective is also to effectively disseminate the results obtained and to provide guidelines to the designers on the best practices for the analog design flow.

The table below summarizes the IP blocks that have been identified as circuits to be developed in the framework of the activity. The status of the development is also shown. In the case of the design of the bandgap, the design was led by an external institute with support from CERN engineers. This model will also be encouraged in the future in order to optimize resources.

ON CHIP REFERENCES	Notes
Bandgap voltage reference and temperature monitor	Block submitted in December 2021. Development led by Bergamo/Pavia with support from CERN engineers.
CONVERTERS	
Digital to Analog Converter (8-bit)	Core block submitted in December 2021. Development lead by M. Piller (DOCT, Austrian programme).
Analog to Digital Converter for monitoring (12-bit)	Design will start in April 2022. Development lead by T. Hoffmann (FELL)
OPERATIONAL AMPLIFIERS	
Rail to Rail Operational Amplifier (Fast)	Completed. To be submitted in 2022. Development lead by J. Kaplon (STAFF)
Rail to Rail Operational Amplifier (slow (e.g. monitoring in unity gain configuration))	In progress. To be submitted in 2022. Development lead by M. Piller (DOCT, Austrian programme)
DATA TRANSMISSION	
Differential line drivers/receivers	IP block submitted in December 2021. Development lead by F. Bandi (FELL)
PLL	
Analog PLL	In progress. Development lead by F. Bandi (FELL). Synergies with Velopix2/Timepix5 projects.
Digital PLL	Design start expected for Q4 2022. Development lead by T. Hoffmann (FELL)

In addition to IP blocks, there are also some proprietary blocks that are being developed and that will contribute to the experience acquired by using the technology. These are front-end blocks for (1) hybrid pixel detectors (such as charge sensitive amplifiers, comparators, threshold adjustment DACs) and for (2) precise timing detectors. In the case of hybrid pixel detectors, the work is done in collaboration with WP1.1. A WP1.1 Fellow (V. Sriskaran) is based at the microelectronics section working with a WP5 master student (S. Emiliani). The joint effort explores the parameter space for the performance achievable with the 28nm technology in terms of time resolution and noise versus power consumption and pixel density for future ASICs like the LHCb Velopix2 or the Timepix5 chips. In terms of precise timing, a circuit for the readout of LGADs has started to be explored (J. Kaplon) and this work will be concluded (M. Piller) in 2022.

In 2022 the design team will participate in the electrical characterization of the first blocks submitted in the technology in the framework of the 5.2a activity (differential driver and receiver and 8-bit DAC). As a part of the dissemination strategy, the team will submit contributions about the circuit designs, their performance and the challenges found with the technology to the TWEPP workshop. The documentation on the blocks and on the process (containing information such as transistor flavours, resistors, capacitors, metal stack, corners, mismatch, etc) will also be released.

A meeting to specifically discuss the technical aspects on 28nm design will be called in order to facilitate designers to share their experiences.

2.3 Rad Tol SoC interconnects

The increase in the complexity of modern ASIC designs in the HEP community and the use of advanced fabrication processes are strong advocators for employing a different methodology in ASIC designs. It would be more productive to follow a more abstract design methodology where the designer will not have to develop fully customized RTL code dedicated to the specific application but instead use pre-existing qualified IP blocks that can be interconnected together utilizing a standardized interconnect. Fully customized RTL code requires as much of a design effort as for verification and when design complexity increases so does the verification effort. Developing a set of IP blocks that are configurable and that adhere to a standardized interconnect bus would enable their reusability in multiple designs and applications. These IP blocks need to be verified only once at the block level and alleviate much of

the verification effort at the top level in the target ASIC application. In industry, a System-On-Chip combines elements of a computer system such as processing cores, memories and peripherals. These elements allow the use of re-programmable functions and algorithms thus increasing further the flexibility of the embedded hardware.

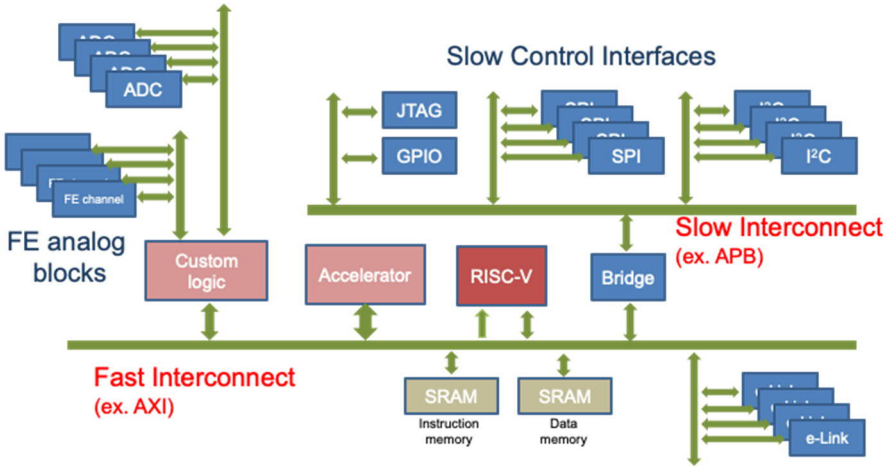

Figure 5. Conceptual block diagram of the Radiation Tolerant System On Chip Ecosystem

Within the WP5 an activity has been initiated focusing on the development of a System-On-Chip Radiation-Tolerant EcoSystem. The EcoSystem will be based on standardized interconnect technologies employing radiation tolerant techniques as well as the preparation of the specifications and of a methodology to develop Radiation Tolerant IP blocks that adhere to the standardized interconnects. A set of example IP blocks is foreseen to be developed. A conceptual block diagram of such SoC Ecosystem is depicted in Figure 5.

In 2021 we have initiated a survey of open source SoC platforms followed by an evaluation of selected platforms. We expect that in 2022 we will be in position to propose a first version of a System-On-Chip Radiation-Tolerant EcoSystem standard for use in the HEP community.

2.4 WP5.2 Powering Solutions

2.4.1 48V rated DCDC converters

A fully working 48V DCDC converter, bPOL48V_V2 has been successfully designed and tested by Pablo Antoszczuk and Stefano Michelis – a remarkable achievement. The converter is designed in the I3T80 OnSemi High Voltage 0.35um technology, a second version of the rad-hard controller (GanC_V2), with some minor modifications compared to V1, adding an Enable line for the 48V linear regulator and modifying it to withstand the Single Event levels for space applications.

This rad-hard controller was integrated in a new version of the buck converter (from 48V to 12V) with GaN power stage, whose resulting board is shown in 6. This board is able to work with both versions of the GaN ASIC from EPC, called EPC2152. There are two versions, with power supplies at 5V and 12V, respectively. With a change of few passive components GaNC_V2 can be configured to provide either 5V or 12V to the EPC2152. This will allow a more flexible integration and the possibility to access to different COTs in the future.

The designed board has been developed in order to be easily pluggable (with only 3 screws) in a reliability testing rack that is under construction (thanks to Maxence Ledoux and David Porret). This rack is designed to host 60 bPOL48V_V2 working at full load (Vout=12V,Iout=12A), with water cooling, in order to test the long term reliability of these objects.

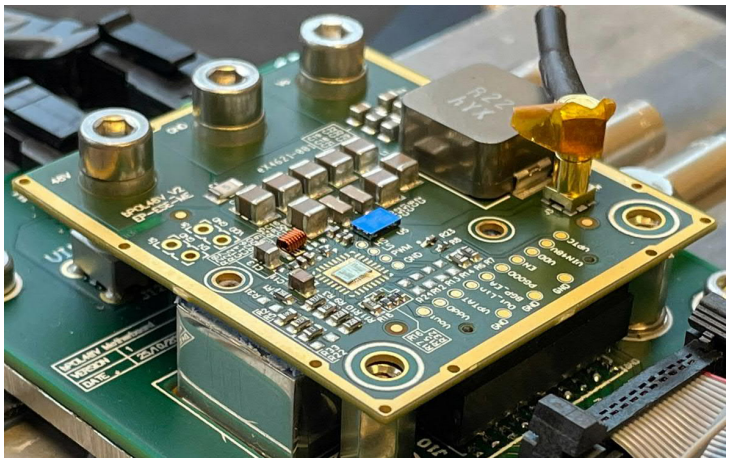

Figure 6. bPOL48V board with the GaNC_V2 mounted on board

During 2021, the first version of the converter (bPOL48V_V1), has been fully radiation characterized The following table lists the maximum dose limits.

TID max	50 Mrad
SEE max	46 MeV/(mg/cm²)
DD max	4e14 n/cm2 2.23e14 p/cm2(30MeV)

The efficiency vs TID is reported in Figure 7. No significant variation is observed up to a TID of 50Mrad.

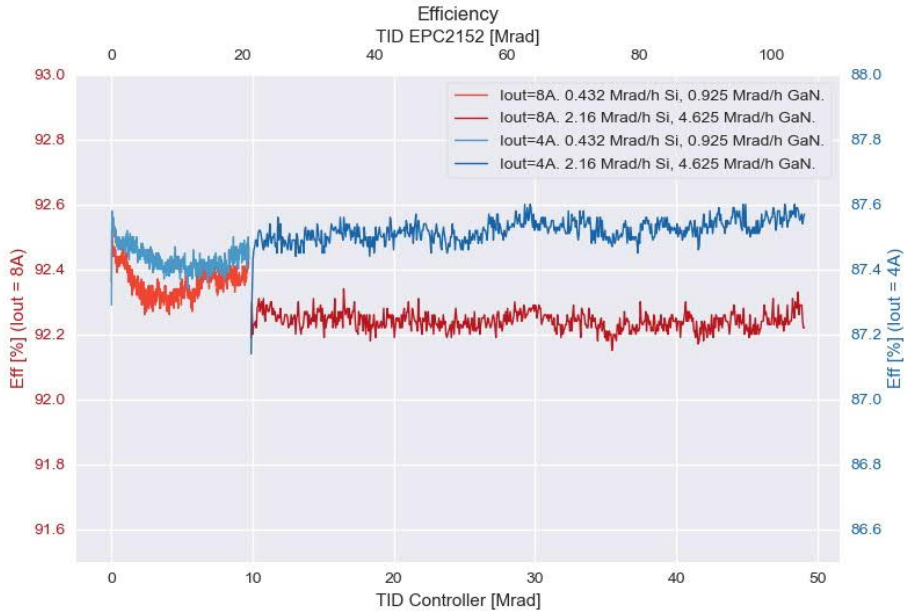

Figure 7. bPOL48V efficiency vs TID. Lower X-axis refers to the TID of the Si-CMOS controller, upper X-axis refers to the TID for the GaN power ASIC EPC2152. The Left Y-axis refers to an output current of Iout= 8A (red line), while the right Y-axis refers to an output current of Iout= 4A (blue line).

When the bPOL48V has been irradiated with Heavy Ions in the CRC facility in Louvain la Neuve, there has not been any damage or long transient in the converter output voltage up to a LET of 46 MeV/mg/cm². The only appreciable variation are small changes in the Vout, below 5% of the nominal output voltage as shown in Figure 8 (for LET=28 MeV/mg/cm²). bPOL48V_V2 is production grade and the controller, GaNC_V2 has been produced in large quantities: 26k dies are today available for use in future experiments and upgrades.

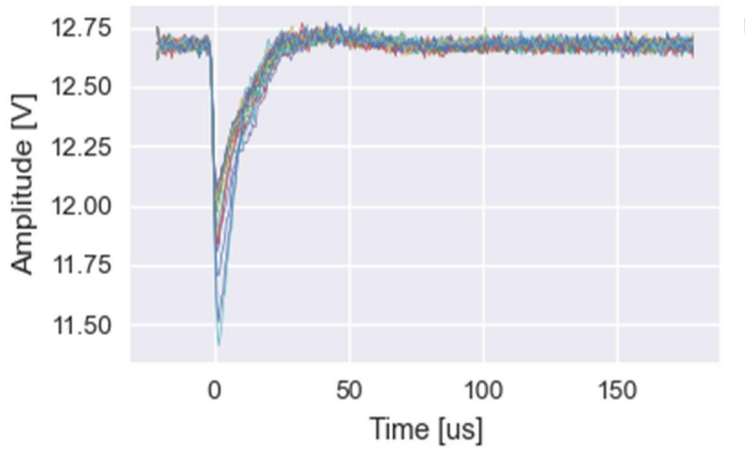

Figure 8. bPOL48V event Vout waveform with SEE hits at LET=28 MeV/mg/cm²

Apart from the development of the bPOL48V, a collaboration with the University of Udine (Italy) has been established in order to explore also other types of architecture for the 48V to 12V conversion. This collaboration has been very fruitful in 2021: a resonant converter, based on Switched Tank architecture, has been designed, produced, and tested. The board design has been carried out by Pablo Antoszczuk, the system simulation by Giacomo Ripamonti (CERN), the design and implementation of the control board and FPGA by Federico Iob and Stefano Saggini from University of Udine. Mattia Balutto (CERN) helped in the integration, simulations with Cadence and particularly in the testing of the object. This converter has been called rPOL48V (r stands for resonant). It is designed with all commercial components, and it is a demonstrator of what can be done in the future for high power density and low profile converters. The difference of size between bPOL48V and rPOL48V are appreciable in 9. It must be noted that bPOL48V is rated only 12A, while rPOL48V is rated 50A, even if it much thinner. The produced board is shown in the Figure 10.

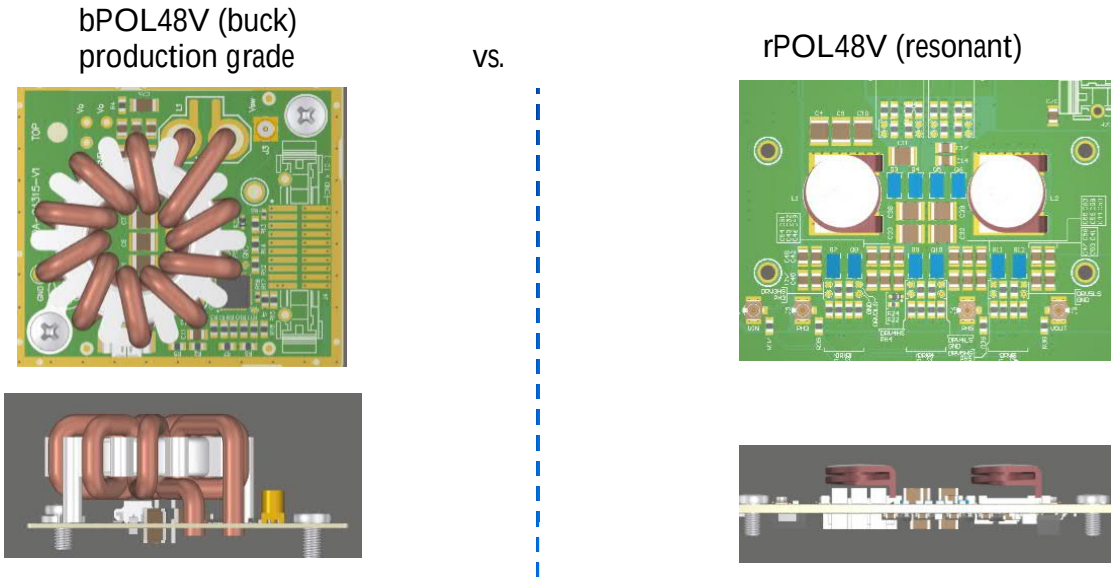

Figure 9. Size comparison of bPOL48V (left) and rPOL48V (right).

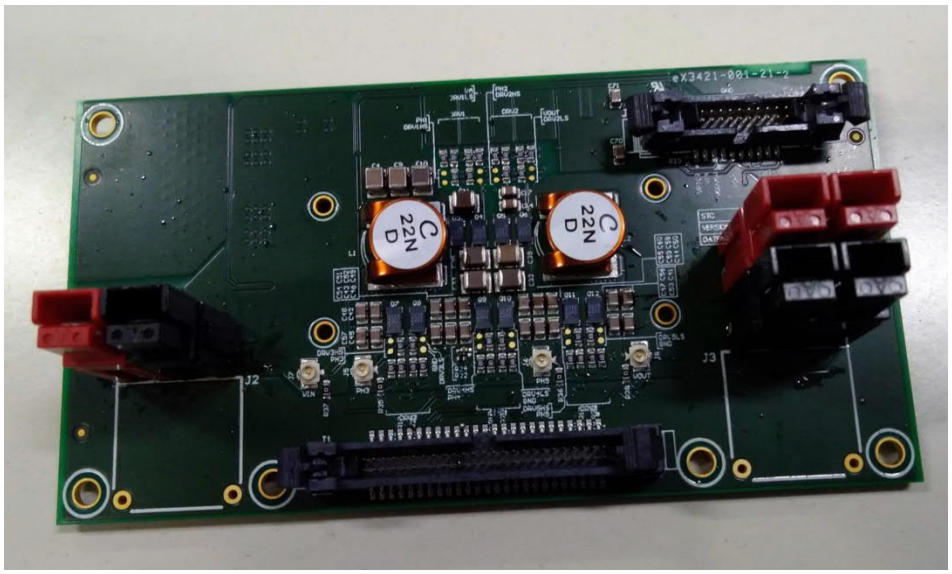

Figure 10. rPOL48V with power connector and testing interface

The efficiency performance of the rPOL48V converter is shown in Figure 11. The peak efficiency is impressive, 97% at 15A (12V output) and 93% for a conversion 48V to 12V and 50A output.

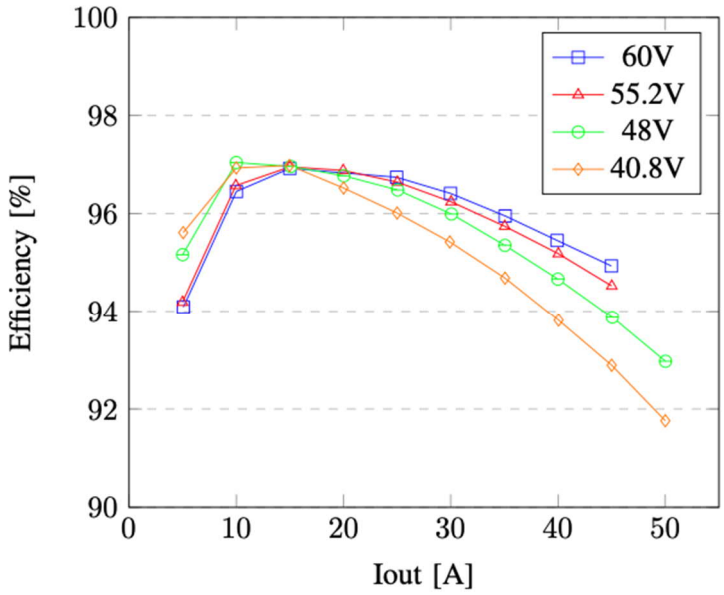

Figure 11. rPOL48V efficiency vs Iout at different input voltages (40.8V, 48V, 55.2V, 60V).

In order to investigate a rad-hard version of the rPOL48V, a fully integrated controller has been designed by Giacomo Ripamonti and Mattia Balutto at schematic level in the OnSemi I3T25 high Voltage technology. At this stage, the layout has still has to be terminated.

In parallel Giacomo supervised the work of two EPFL students (Leo Johansson and Nicolas Galante) for the design of a chipset (composed by three different ASICs) to drive a commercial GaN transistor. This chipset, called DrGan (DRiver GaN) is today in production and will be tested in 2022.

In addition, since the OnSemi I3T80 technology which was used for the design of the GaNC ASIC is becoming obsolete, it is mandatory to find another HV technology for the design of future DCDC converter. Hence a set of test chips have been designed and produced in the OnSemi I4T technology, that provided devices at 15V, 30V, 45V and 70V.

2.4.2 28nm fully integrated Point of Load converter

This activity was not part of the initial plan of the WP5.2, however it emerged from discussion with the digital designers in the ESE-ME section. It became clear that on-chip regulation for the supply voltage in the 28nm technology would be a clear asset for the design of future front end ASICs.

In this context two different activities have been started, aiming at radiation hardness in the 1Grad domain:

- Design of a Low-DropOut linear regulator (LDO): Stefano established a collaboration with the University of Graz (Austria) for the development of such a device with the following specifications: Vin=1.2V, Vout=0.9V, Ioutmax=200mA. The schematic design is ongoing: pass transistor dimension has been selected and stability analysis for the amplifier is ongoing. Finalization of the LDO is foreseen during 2022.
- Design of a fully integrated DCDC converter: the full DCDC converter design team (Stefano, Giacomo and Pablo) in collaboration with the University of Udine worked on the definition of a resonant DCDC converter architecture that is able to provide a conversion ratio of 4, fully integrated, meaning that also all the passive components are inside the ASIC. The switching frequency is around 200MHz and the inductors available in 28 nm technology will be used. The

main specifications are: Vin=4V to 5V, Vout=0.9V, MaxIout=250mA. The design just started and a first prototype will be available in 2022.

3. Publications and contributions to conferences and workshops

P. Antoszczuk, S. Michelis, G. Ripamonti, S. Saggini and F. Iob "48 V input rad-hard DCDC converters for HEP experiments: development and results"2022 JINST 17 C01068

References

[1] 1st 28nm Technology Forum, Thursday 12 Nov. 2020 https://indico.cern.ch/event/970389/

[2] 2nd 28nm Technology Forum, Thursday 10 Mar. 2021, https://indico.cern.ch/event/1009040/

[3] 3rd 28nm Technology Forum, Monday 28 June. 2021, https://indico.cern.ch/event/1042567/

[4] 4th 28nm Technology Forum, Wed. 23 March 2022, https://indico.cern.ch/event/1132318/

WP6 High Speed Links

1. Introduction

Anticipating the bandwidth requirements of future HEP detectors, with embedded electronic and optoelectronic systems operating in intense radiation conditions, WP6 aims at the demonstration of low power, radiation tolerant components that are capable of bandwidths in excess of 50 Gbps/lane[8]. Moreover, such systems should follow industry standards by employing Commercial Off-The-Shelf (COTS) FPGAs and optoelectronic transceivers so that backend systems can be designed without resorting to ad hoc developments. Figure 1 illustrates the roadmap for WP6. Current systems installed in the LHC detectors support data rates of 10 Gbps with radiation tolerances up to 1 MGy and 10^{15} n_{eq}/cm^2. The objective of WP6 is to demonstrate the feasibility of systems operating at 56 Gbps/lane, or 224 Gbps per fibre with Wave Division Multiplexing (WDM), while being capable of sustaining 10 MGy and 10^{16} n_{eq}/cm^2 radiation.

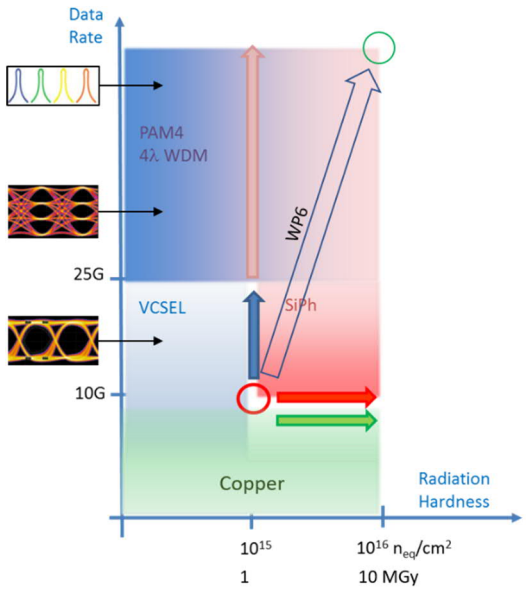

Figure 1: Evolution towards higher data rates (in bps) and radiation hardness.

WP6 addresses the three areas necessary to work towards this goal: the ASICs activity studies high-speed transmitters using higher order modulation signalling and advanced CMOS technologies (28 nm). The FPGA activity keeps track of the evolution of the industrial standards, sets up laboratory demonstrators with state-of-the-art systems and develops test benches for the WP6 custom developments. Finally, the OPTO activity develops radiation-hard optoelectronic components with the aim to demonstrate a Silicon Photonics (SiPh) radiation-hard data transmission system. The OPTO activity strives also to develop physical models of radiation damage in optoelectronic components in order to guide the development of new devices.

Figure 2 embodies the WP6 system vision, presented at the EP R&D Day 2021 [1]. A clear distinction is made between embedded detector systems and counting room (backend) systems. In the counting room, the development is based on COTS electronic and optoelectronic components since very low radiation doses are expected at those locations. Special emphasis is put on FPGAs to build the system and it is additionally proposed to keep the radiation sensitive laser diodes in the counting room. The lasers installed in the counting room will be the light sources of WDM systems that effectively multiply the fibre bandwidth by the wavelength-multiplexing factor used (four in the figure). For the on-

[8] Lane: single wavelength in a wavelength division multiplexed system

detector systems the opposite strategy is used, that is, the systems are custom made and qualified to resist radiation. These include data communications ASICs: data aggregators, PIN-receivers, modulator drivers and the SiPh optoelectronic components: ring modulators, PIN-diodes and waveguides.

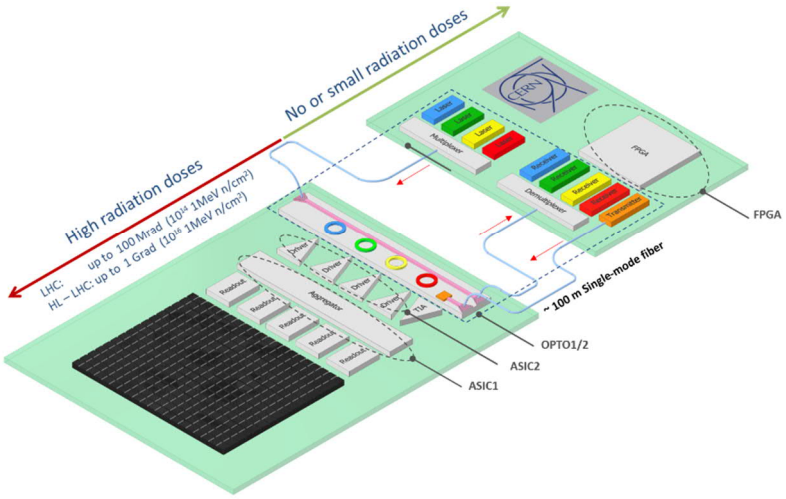

Figure 2: HEP SiPh data transmission system.

The ASIC activity has started with a year's delay (2021). It is currently supported by a PhD student, Adam Klekotko (from March) and two fellows: Mateusz Baszczyk (from April) and Stefan Biereigel (from October). The FPGA activity is supported by a fellow, Chaowaroj Wanotayaroj. Finally, two PhD students, Milana Lalovic and Thenia Prousalidi work on the OPTO activity.

2. Main activities and achievements in 2021

The year 2021 saw progress in the three WP6 activities and, in particular, it was the starting year for the ASIC activity. That led to the definition of the architecture of a 28 Gbps transmitter chip demonstrator and allowed the detailed circuit design to start, aiming at the fabrication of a prototype during 2022. The FPGA activity remained a cornerstone of WP6 with studies of the data-communications market and, in particular, the evaluation of Forward Error Correction (FEC) codes that are considered unavoidable for error free data transmission in systems that use higher order signalling, e.g. PAM-4. Impressive progress has been made by the OPTO activity with the demonstration of radiation hardness in electronics devices up to 10 MGy TID and 3 x 10^{16} 20 MeV n/cm^2 NIEL. These components include a modified (for radiation hardness) ring modulator and a germanium photodiode (PD). Both components were used to demonstrate data transmission with the Ge PD used to implement a 5 Gbps receiver and the ring modulator used to produce a clean NRZ eye-diagram at 25 Gbps.

3. FPGA-1: FPGA-based system testing and emulation

After the previous phase of setting up the laboratory followed by a review of the standards and key figures of merit, the FPGA-1 activity was dedicated to implementing COTS-based PAM-4 and NRZ-28 systems during 2021. These were compared to typical HEP use cases in order to guide the ASIC and OPTO activities of WP6. Investigations of line rates as well as different FEC and line-coding schemes were carried out and compared to the availability of COTS transceivers. Full details were reported at TWEPP by Chaowaroj Wanotayaroj [2] and an overview is given below.

Implementation and evaluation of a full PAM-4 link with typical FEC and COTS

The tests of 28 Gbps NRZ and 56 Gbps PAM-4 links performed during 2020 on electrical and optical physical layers confirmed the noisy nature of the optical layer and emphasized the need of strong

Forward Error Correction (FEC) schemes to reach the errors rates of 10^{-9} or below typically required by HEP experiments. This is especially important for the PAM-4 modulation scheme, which comes with an 11-13 dB Signal-to-Noise Ratio (SNR) penalty.

Potential candidate FEC schemes were therefore identified for our applications among standards-based links and error-correcting code families known to be efficient in the HEP environment (in particular Reed-Solomon (RS) codes) and were studied for further implementation. Mathematical modelling of custom FEC candidates for 56 Gbps PAM-4 was carried out to assess their respective coding gains. The model was compared to the IEEE one to check its validity. Once validated, our model enabled the comparative analysis of the performance of future RS-based FEC schemes to determine the impact of various key parameters (symbol number and size, correction power/complexity). Some examples are shown in Figures 3 and 4.

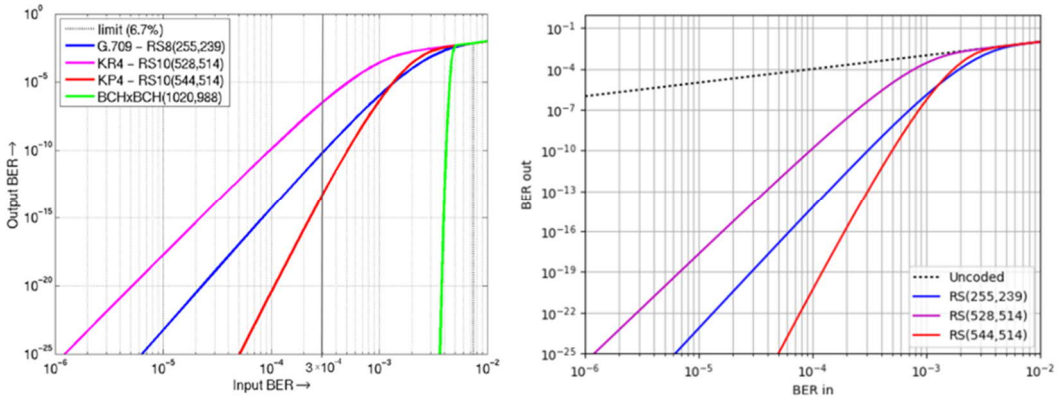

Figure 3: Coding Gain of various FEC types (left: IEEE, right: WP6 model).

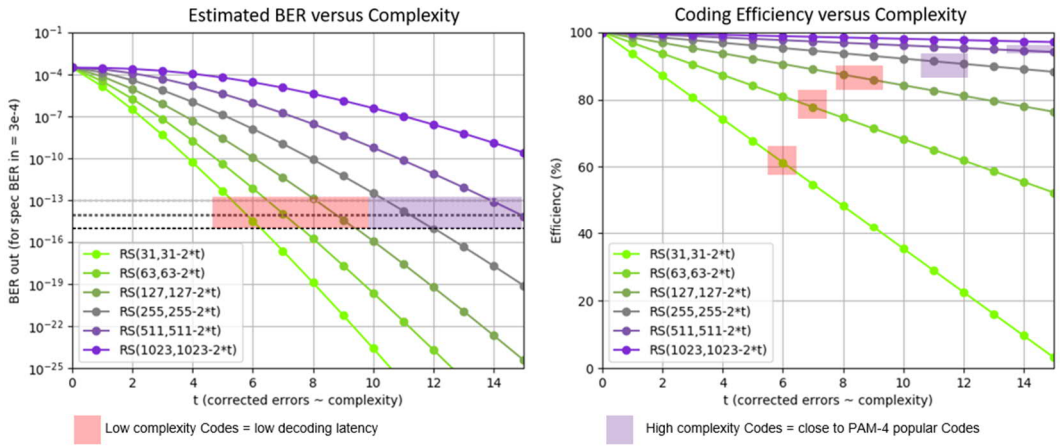

Figure 4: Reed-Solomon efficiency estimation versus complexity according to the WP6 model.

As no specific FEC is imposed by current PAM-4 standards, a pragmatic choice was made for the first proof-of-concept: the implementation of the KP4-RS10(544,514) code which is based on a Reed-Solomon RS(544,514)[9] encoding scheme and that is able to correct 15 symbols of 10 bits each in a 544 bit-frame. This choice was guided by several factors:

[9] The standard notation for Reed-Salomon codes is RS(N,K) where N is the total number of symbols in the message, K the number of symbols to be encoded and N-K the number of Forward Error Correction (FEC) symbols. The error correction capability is t=(N-K)/2 symbols and the symbol length in bits is $\log_2(N+1)$.

- Popularity: according to the *Implementation Agreement* created and approved by the Optical Internet-working Forum, the IEEE KP4 scheme is currently under consideration by several standards bodies for electrical PAM-4 interfaces;
- Complexity: this scheme is very powerful and allows correction of up to 15 10-bits symbols;
- Efficiency: the estimated coding gain of KP4 is 6.1dB, better than its competitors;
- Practical Implementation: both Intel and Xilinx are proposing a hardcoded KP4 FEC IP integrated in their transceiver block. This has the big advantage of removing the in-fabric resource usage in the FPGA, which can be substantial for FEC encoders and decoders;
- Decoding Latency (often a consequence of complexity) is also an important figure of merit and is not a strength of the KP4 scheme. This was evaluated on our proof-of-concept but was not considered as a showstopper.

A full link, emulating both the transmission (ASIC) and the reception (Back-end) sides, has been implemented using custom firmware, IP blocks from the FPGA manufacturer (for example featuring the transceiver and the KP4 FEC encoder/decoder) and commercial optical transceiver modules. A full optical loopback was studied, its coding gain was assessed (see Figure 5 below) and its latency measured to be 460 ns including a few meters of fibre. It is worth noting that the large size of the KP4 frame is already responsible for 97 ns latency, even without considering the decoding process.

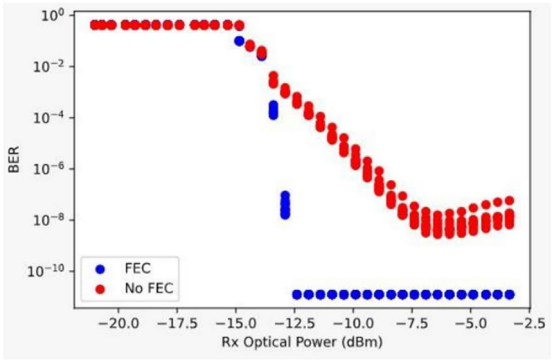

Figure 5: Bit Error Rate of the KP4 PAM-4 link implemented in WP6 proof of concept. For the FEC case and optical powers above -12.5 dBm, the limit error rate (1/number of error free transmitted bits for the duration of the measurement) is given.

Line rate study

In order to allow data transmission synchronous to the LHC collision rate (40.079 MHz), a PAM-4 link would need to be operated at a non-IEEE standard rate (which is 53.125 Gbps). A study was therefore performed on FPGAs and available transceivers to address the feasibility. The results of this analysis (see Figure 6) concluded that, although FPGA transceivers seem to tolerate large rate variations, the optical transceiver modules we had only accept a very narrow range of data rates (< ±500 ppm) which does not cover any integer multiples of the Bunch Clock frequency (i.e. 1325 or 1326 times 40.079 MHz). The frequency range limitations of the optical transceiver modules preclude the traditional approach in HEP of using synchronous systems operating at a multiple of the bunch clock frequency.

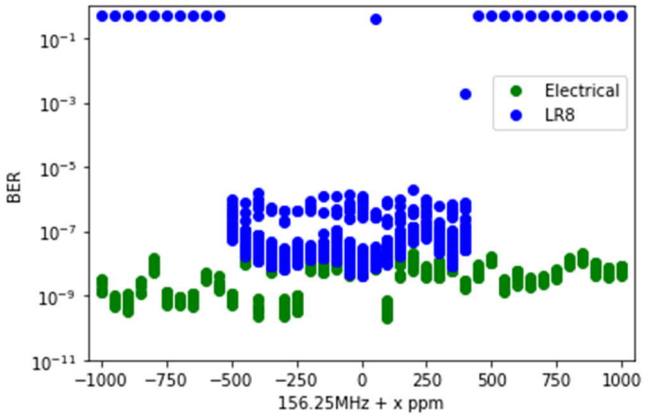

Figure 6: Locking range of Virtex Ultrascale+ GTM transceiver (green) and PAM-4 LR8 module (blue).

- To quantify the limitations and find ways to circumvent these limitations the following studies were carried out:The development in VHDL of a bunch-clock synchronous interface model for a disruptive link type based on asynchronous PAM-4 transmission. This solution was fully simulated as a proof-of-concept, and the complexity of implementing it in an ASIC is being evaluated.
- A market study of available optical transceivers, both for NRZ-28 and PAM-4, with the objective to identify modules that allow their Clock and Data Recovery (CDR) circuits to be bypassed. During this study, the availability of these modules on the C-band (around 1550 nm) was also assessed to address a concern of the OPTO activity. The results are shown in the next section.

PAM-4 and NRZ-28 market study

The market is still evolving and standards are being published every quarter. Early adopters (Amazon, Facebook etc.) often purchase products which are not yet standardised and manufacturers have two parallel paths of development, one quickly moving path for these early adopters (no interoperability is therefore guaranteed for these products) and another one, at a slower pace, to match the IEEE standardization procedures.

A technical survey performed in 2021 on the current market situation of commercial optical transceiver modules for NRZ-28 and PAM-4 with in-depth analysis of the parameters important for the other WP6 activities (wavelength, data-rate, retimer bypass capability) led the following observations:

- PAM-4 market: no commercial module providing PAM-4 modulation allows operation at a multiple of the LHC bunch clock frequency. Due to the challenging requirements, retimers are crucial and cannot be bypassed, requiring a working range of ~ ±500 ppm (53.125 GHz ± 26 MHz). Asynchronous transmission would therefore be unavoidable. Moreover, the complexity of the FEC scheme required to reach a target error rate of 10^{-9} or below is very high. The price to pay in FPGA resources in order to implement a custom scheme would be extremely high. This would force the use of hardcoded FEC types like the KP4, coming with potentially penalizing long frames and large latency. Finally, PAM-4 commercial optical transceiver modules are expensive and symmetric structures, when typically only the receivers would require PAM-4 modulation in the case of the Back-end electronic systems of HEP detectors.
- In the other hand, the NRZ-28 market is more flexible. Retimers can often be bypassed, opening the door to synchronous transmission. FEC can also be lighter, thus limiting the

latency and complexity of the implementation and there is more room for asymmetric and less expensive solutions.
- On the wavelength front, most PAM-4 and NRZ-28 transceivers are provided in the O-band (~1310 nm). Very few are available on the C-band (~1550 nm).

These observations allowed the ASIC and OPTO activities to steer their objectives for 2022:

ASIC: The ASIC-1 and ASIC-2 activities will focus first on an NRZ-28 Gbps demonstrator, the DART28, which will be a first step in a series of iterative designs, demonstrating an evolution of high-speed links for future experiments and could reach 100 Gbps when associated with a CWDM4 Photonic Chip.

OPTO: although the current PICv2 device is conveniently equipped with several 1550 nm ring modulators on the same waveguide and it could benefit from the availability of erbium-doped fibre amplifiers (*EDFA*), it may be required to increase the number of O-band structures in the upcoming PICv3 development to ease interoperability with Back-end COTS targeting ~1310 nm Ethernet applications.

Implementation of a full NRZ-28 link DART28 compatible based on COTS

In order to accompany the design of the DART28, a full NRZ-28 Gbps link, fully compatible with the DART and implementing its FEC was designed and evaluation has started with a NRZ-28 Gbps transceiver with retimer bypass possibility.

4. ASIC Activity

Tasks 1 and 2 within the ASIC activity address the design of very high data-rate transmitters and driver circuits for Silicon Photonics Modulators in advanced CMOS technologies. The project draws on the use of a 28 nm CMOS technology and aims at developing a 28/56 Gbps transmitter, comprising a serializer, a low-jitter PLL, cable and ring modulator drivers (NRZ and PAM-4).

The first prototype, to be summited for fabrication during 2022, will operate at 25.65 Gbps NRZ (a multiple of the 40.079 MHz LHC Bunch Clock frequency) and will be capable of driving 100 Ω transmission lines and ring modulators like the ones on the Photonics Integrated Circuit (PIC) developed at CERN. The chip (the DART28) will use NRZ signalling.

During 2021, the chip architecture was defined and it is (partially) represented in Figure 7. It consists of a Pseudo-Random Bit Sequence (PRBS) generator (not shown in the picture), the data path (comprising the scrambler, the Forward Error Correction (FEC) encoder and the interleaver) and the output driver. The data, generated by the PRBS generator, are encoded and then fed to the serializer that operates as a 640-to-1 time-division multiplexer. The serial data stream is then driven off-chip either through the cable driver or the ring modulator driver. It should be noted that the chip is not capable of receiving user data. This was a choice taken to simplify the first prototype and thus to allow a short development cycle of the demonstrator ASIC. In this way, emphasis is put on the development of the critical elements of the transmitter leaving the user interface (of a more standard nature but time consuming to design) to a later stage.

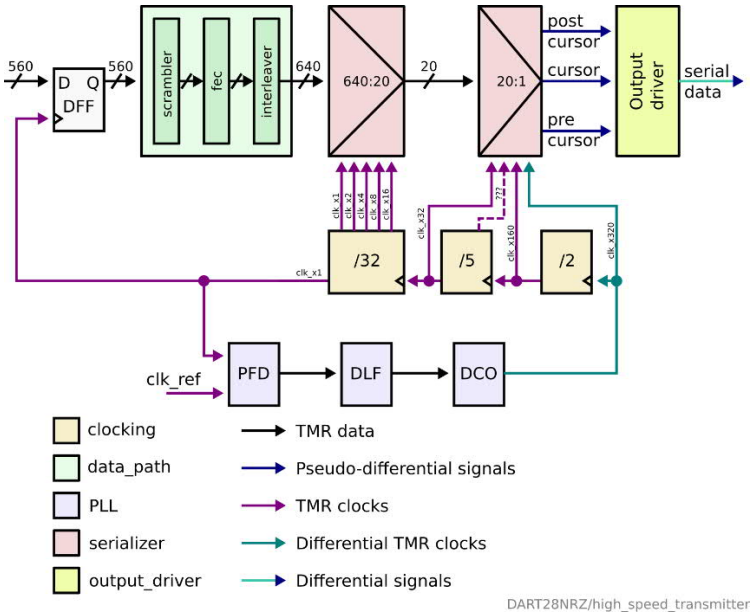

Figure 7: DART28 ASIC architecture.

The serializer is based on a half-rate architecture. It is thus required that the PLL generates a 12.8 GHz clock signal, and its sub-multiples, to drive the serializer. Transmission at such high data rates requires the clock jitter to be below 1 ps. To achieve this performance an LC oscillator using an "All"-Digital Phase-Locked Loop (ADPLL) architecture was chosen.

Particular challenges on this design are the control of the duty-cycle of the fast signals to minimize jitter at the output of the serializer, plus the driving of the SiPh ring modulator with the low voltages compatible with the supply voltage of the 28 nm CMOS technology used. To overcome this limitation (and thus maximize the driving amplitude) the ring modulator is driven pseudo-differentially on both the anode and cathode terminals. This, however, might lead to the PN-junction of the ring modulator being forward biased, which must to be avoided. To accomplish this, the driver was designed to produce asymmetric (and programmable) amplitude signal swings on the anode and cathode terminals.

During 2021 schematic level design of the various components (except the APLL) was done and the synthesisable RTL code written. The designers have now moved to the layout phase of the full-custom circuits.

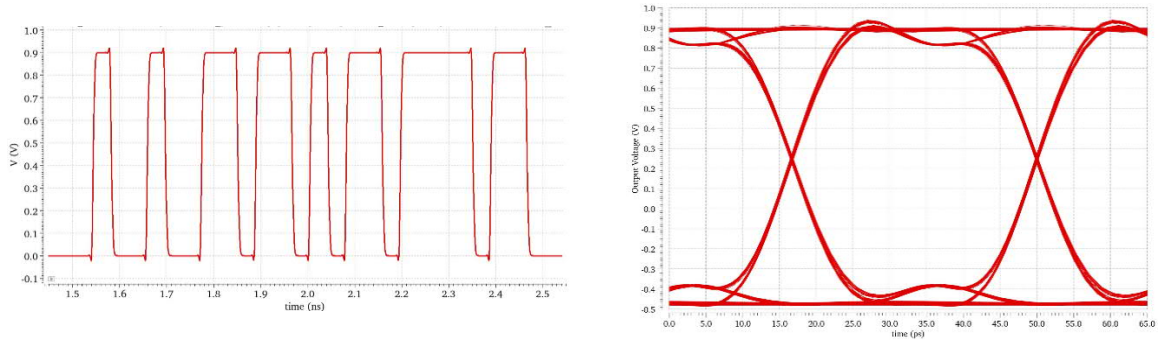

Figure 8: Simulation results: Serializer output (left), ring modulator driver output at 25.6 Gbps (right).

5. Silicon Photonics

The Silicon Photonics activity has progressed in 2021 by further exploiting the test structures available on PIC v.2, both in a standard lab environment through functionality measurements and in irradiation tests. Functional testing has demonstrated two important features: operation at 25 Gbps as well at 25 GBaud PAM-4, tests made with a commercial line driver and newly available test equipment; as well as a proof of principle for the ring modulators being driven directly by the outputs of existing ASICs thus paving the way for tighter integration between future FE ASICs and the optical links.

System and Chip development

Using the various devices present on PIC v.2, progress has been made on further understanding of the thermal control of ring modulators, integration with existing FE ASICs for early system demonstrators, and proof of concept operation at 25 Gbps NRZ and 25 GBaud PAM-4.

Silicon micro-ring modulators are very sensitive to design and temperature variations, since the resonators have rather high Q-factors. This means that the local device temperature has to be tightly controlled in all practical applications. In order to study this further, a test setup based on a computer-controlled feedback loop has been built. PIC v.2 has several test structures where the ring modulator has a drop port from which a small fraction of the light circulating in the ring is bled into a waveguide connected to an integrated germanium photodiode that can be used to monitor the amount of DC light in the ring (see Figure 9). These test structures also have tungsten heating elements patterned above the active regions of the rings that can be used to raise the temperature of the ring in a highly-localized way by passing a current through them. By injecting broadband light into the bus waveguide that the ring sits on, one can observe the change in resonance wavelength as the local device temperature is controlled with the resistive micro-heater (see Figure 9) [3].

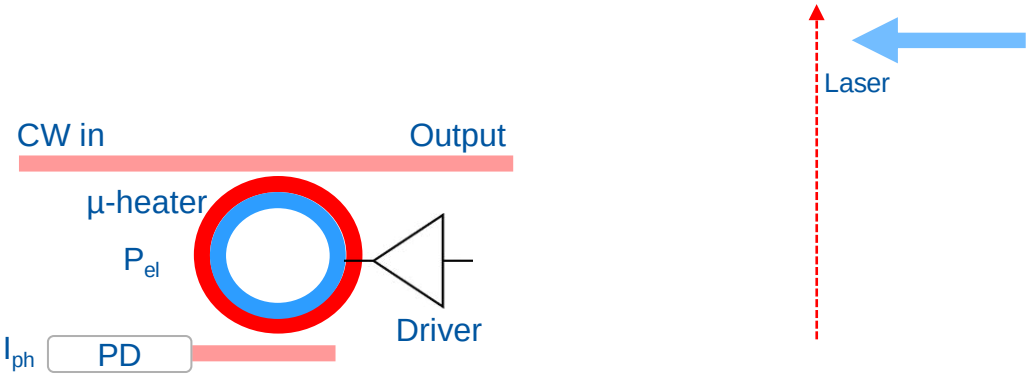

Figure 9: (left) schematic of micro-ring modulator with heater and drop port with photodiode; and (right) demonstration of the effect of changing the ring temperature on the optical transmission spectrum: by lowering the heater temperature the resonance can be moved in the direction of the horizontal blue arrow to overlap with the input laser wavelength represented by the vertical red arrow.

In order to lock the ring modulator to the input wavelength, it is necessary to implement a control loop to drive the heater current based on feedback from the drop port photodiode. Eventually this control circuit will be integrated into the modulator driver and therefore the controller parameters need to be determined. A test bench was set up, based on laboratory instruments, to drive the heater current and monitor the photocurrent in the photodiode, with a PID controller implemented in software on a computer controlling the instruments. Figure 10 shows the schematic and performance of the controller, which is being used to define the controller coefficients for the future integration of the controller in a driver ASIC.

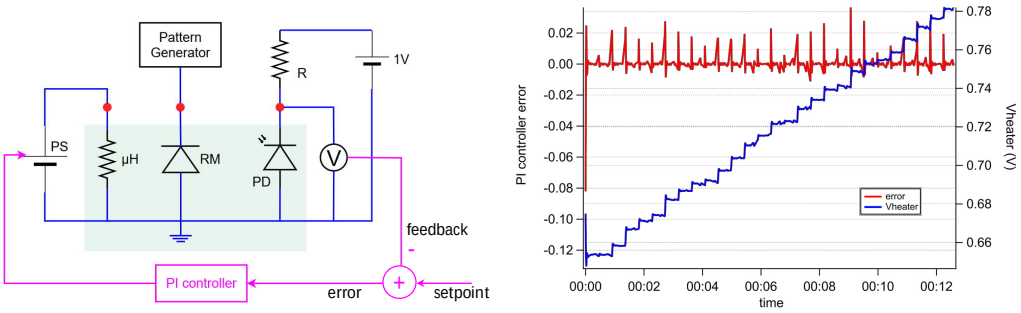

Figure 10: (left) Schematic of the Ring Temperature controller; and (right) Error signal and heater voltage output of the controller as the input wavelength is scanned, showing good tracking of the controller to keep the ring locked to the input wavelength.

Early system demonstrations are important to show feasibility of this technology in realistic conditions. To this end, a ring modulator on a test board was driven directly from an existing lpGBT chip as shown in Figure 11. We observed that standard CML outputs do provide sufficient drive strength at 10 Gbps to build a functioning link even without optimization [4]. For the control path, an integrated germanium photodiode with polarization diversity input was integrated with the existing GBTIA chip to build a first demonstrator. This was also successful, achieving a sensitivity at 2.56 Gbps of -10 dBm at 850 nm. These demonstrations were reported in an oral contribution to TWEPP 2021 by our doctoral student Thenia Prousalidi [5].

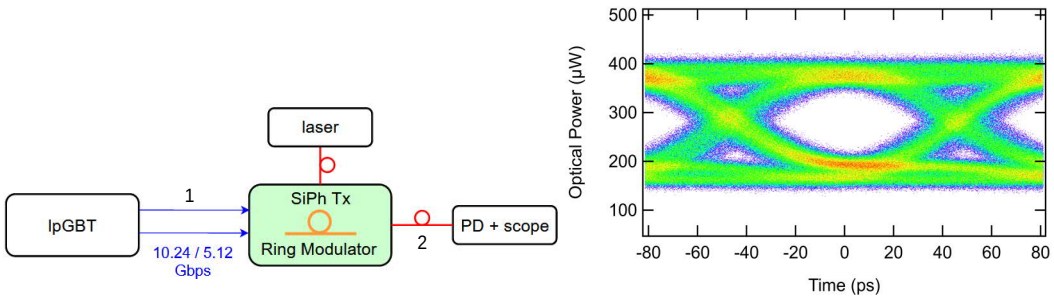

Figure 11: TX demonstrator based on lpGBT (left) and output eye diagram at 10.24 Gbps rate (right).

The group was able to purchase at high-speed pattern generator and checker in 2022. This instrument allows the generation of arbitrary data patterns for both NRZ and PAM-4 at rates up to 28 GBaud. With this instrument as pattern generator, we were able to operate a commercial retimer chip as proxy for a modulator driver and show that operation of the prototype ring modulators is feasible at the WP6 target maximum rate of 25 GBaud PAM-4, as shown in Figure 12.

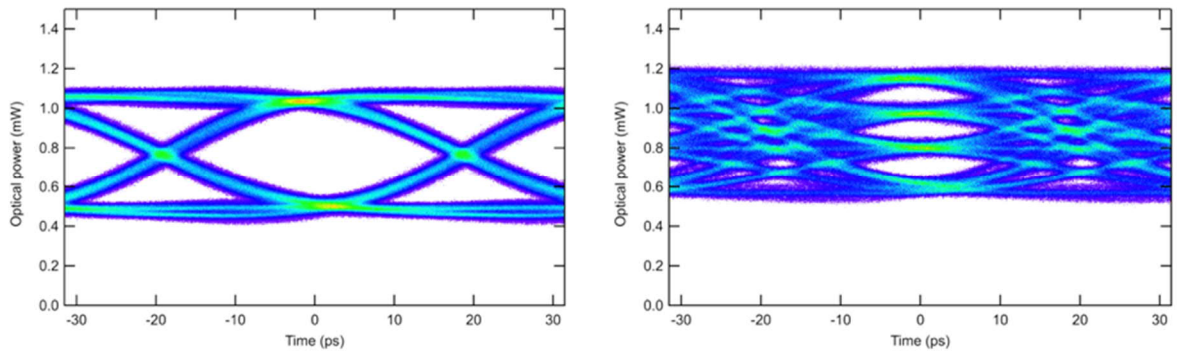

Figure 12: Operation of a ring modulator driven by a commercial driver at 25 Gbps NRZ (left) and 25 GBaud PAM-4 (right).

Thanks to collaboration with the Optoelectronics Research Centre (ORC) at Southampton University (UK), we were able to demonstrate a world first in 2021: coupling of a hollow-core optical fibre to a Silicon Photonics PIC. The hollow-core Nested Antiresonant Modeless Fibre (NANF) was made available by ORC and prepared in our lab for coupling to PIC v.2. Measurements were carried out that showed that, although there was some additional loss as expected from the different mode field diameter of the NANF compared to standard fibre, we were able to successfully couple the fibre to the PIC and transmit data at 25 Gbps. Since the light is guided in air in a hollow core fibre, as the name suggests, this type of fibre has been shown to be significantly more radiation tolerant than standard fibres guiding light in glass. Our experiment thus paves the way for an assembly that would have the ultimate radiation tolerance. These results were accepted for an oral presentation by Carmelo Scarcella at OFC 2022 [6].

Radiation Hardness

Two major radiation effects studies were carried out in 2021: the first a neutron irradiation aiming to explore the ultimate radiation tolerance limits of the germanium photodiodes; and the second an X-ray irradiation to study the impact of device operating temperature on radiation tolerance. Both studies were carried out on the devices fabricated on PIC v.2.

The neutron irradiation test was carried out at the neutron beamline at the UCL cyclotron in Louvain-la-Neuve, Belgium, in May 2021. The five different photodiode designs present on PIC v.2 were irradiated to a total fluence of $3x10^{16}$ n/cm^2. As shown in Figure 13, the best performing devices are a factor of ten more resistant than the discrete InGaAs photodiodes used in optical link systems so far and approximately a factor of two more resistant than the integrated germanium photodiodes tested previously. This is very promising for the overall radiation tolerance of a full Silicon Photonics transceiver for the highest future radiation-level applications.

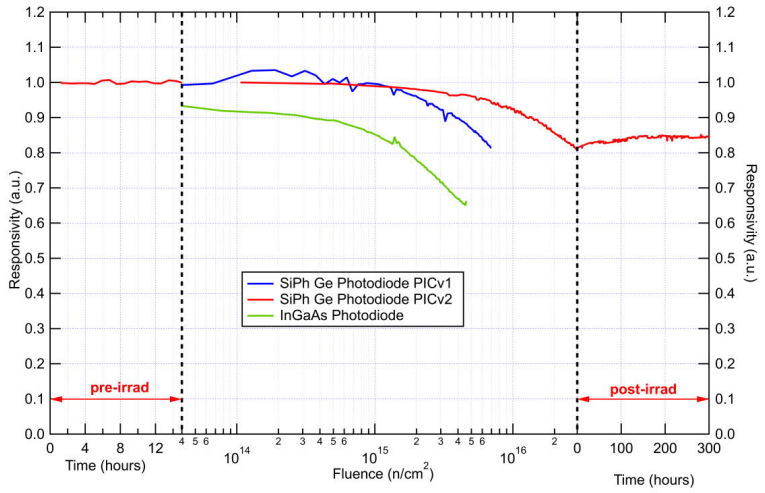

Figure 13: Radiation-induced change in responsivity of integrated germanium photodiodes.

The X-ray irradiation carried out in April 2021 allowed us to evaluate the impact of temperature on the radiation effects. The built-in heaters on each ring modulator were used to set the device temperature to different values during irradiation. The irradiation was carried out at CERN and a total dose of 11 MGy was reached. As shown in Figure 14, the temperature appears to have a non-linear effect on the overall radiation response, with both high- and low-temperatures being beneficial compared to intermediate ones. The fact that the higher temperatures are not detrimental to the radiation tolerance is excellent news for the overall system performance as it means that we will be able to use thermal tuning to stabilise the ring modulator as described in the previous section without having the concern that this will negatively impact the radiation tolerance. These results were reported as a

poster contribution to the RADECS 2021 conference by doctoral student Milana Lalović and accepted for publication in IEEE Transactions on Nuclear Science [7].

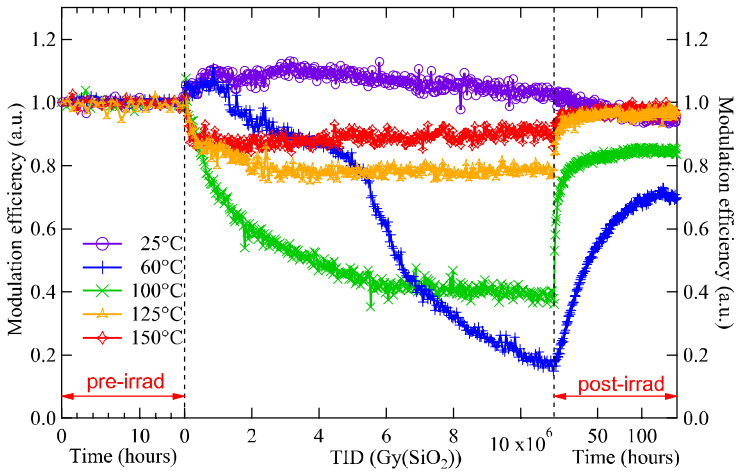

Figure 14: Impact of temperature on ring modulator radiation response.

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WP7 Software

1. Introduction

In the Software Work Package, we focus on areas where increases in efficiency and improvements in performance will enable future experiments to maximise their physics return and reduce the overall time-to-results of physicists doing analysis. The R&D WP consists of tasks which will speed-up accurate *simulation*, optimise event *reconstruction* in modern detectors, improve *analysis* throughput and deliver well tested and coherent *software stacks* to experiments. All this is centred in the new hardware landscape of *heterogeneous computing*.

The software work package of EP R&D reached its full complement of fellows in 2021, with substantial progress being made in all of the task areas. The group held regular meetings throughout the year, helping to maintain its sense of identity in what was still a challenging period, due to the ongoing pandemic. Each task presented at least twice on their progress, as well as having two contributions from the group to the EP R&D seminar series (Turnkey and Tracking tasks).

In addition to the ILC, CLIC, FCC and CEPC communities, progress was made on collaboration with other high-energy and nuclear physics projects. We established strong links to the EU-funded AIDAinnova work package on Software for Future Detectors; and with the EIC ATHENA proto-collaboration, who use the turnkey software stack and ACTS tracking components. These discussions will continue in the coming year.

2. Main activities and achievements in 2021

2.1 Turnkey Software Stack

The turnkey software stack (Key4hep) will provide a complete data processing solution for simulation, reconstruction, and analysis for high energy physics detector studies. It is based on established solutions Gaudi [1], DD4hep [2], ROOT [3] and Geant4 [4]. The event data model (EDM) developed for Key4hep is EDM4hep, which is created with the PODIO EDM framework [5, 6]. As part of the EP R&D project the software frameworks for the CLIC and FCC detector studies are being merged into this Turnkey Software Stack. This stack is also used as a testbed for the other developments in the EP R&D project, not only the software developed in this work package – ACTS, CLUE as described below – but also to enable a feedback loop between hardware developments, such as silicon sensors or noble liquid calorimeters and detector design studies

Build System, Deployment and Infrastructure

2021 has seen more than 25 (minor) releases of the Key4hep software stack, reflecting the rapid pace of development. The build system, based on the HPC package manager Spack [7], was initially developed in 2020, and has met the needs of the turnkey software stack in providing a flexible and efficient way to build and deploy. Via deployment to CVMFS, the turnkey software stack is immediately available on CERN batch and grid resources, as well as services such as SWAN. Maintenance of the package recipes has allowed all packages to be built with a wider range of compilers (gcc 11, clang 12) and provides a robust way of reproducing old builds. Several generators (KKMCee, BHLumi, BabaYaga) are among the new packages added to the stack. By including k4CLUE and ACTS, the common infrastructure has also helped the synergies of the turnkey software stack with the other software products described in this chapter.

Adapting FCC Software to the Turnkey Software Stack

The FCC software framework FCCSW, which supported full detector simulations for the FCC Conceptual Design Report, used similar underlying libraries and technologies to Key4hep, in particular the Gaudi framework and the PODIO data model library. The work of achieving a deeper integration of FCCSW in Key4hep, which started at the end of 2020, has thus not faced significant technical obstacles, but the extensive codebase required the repositories to be re-organized to allow the sharing of non-FCC-

specific components between other Key4hep participants; this has already improved maintainability and robustness of the turnkey software stack by sharing the burden of maintenance. Specifically, the core repository and those supporting generation, simulation and calorimeter reconstruction were restructured [8].

Adapting the CLIC Software to the Turnkey Software Stack

To integrate iLCSoft algorithms, which were developed for ILD studies, but run in the Marlin framework, into Key4hep, a wrapper was developed that provides the necessary converters and interfaces: k4MarlinWrapper. This instantiates the Marlin processors to be run through Gaudi algorithms; the source code remains unchanged. To enable a smooth integration, k4MarlinWrapper includes an in-memory converter between the different Event Data Models and a converter script for the configuration input file that supports execution markers and parsing of constants. Using the k4MarlinWrapper, one is now able to execute multiple events in parallel with LCIO input by adapting its input reader and output writer to their multi-threaded versions, adapting the processors where needed, and using Gaudi to orchestrate the execution. There is ongoing work to expand the parallel execution to be used with EDM4hep input with the latest PODIO developments.

The conversion of the supported EDMs is performed in-memory and on-the-fly: conversions between both LCIO and EDM4hep can be configured on a per-algorithm basis, indicating the selected collections to be converted both on input and output, as depicted in Figure 1. The conversion from EDM4hep to LCIO is set to be used for input so that the underlying Marlin processors get the input in the expected format. Conversion from LCIO to EDM4hep is set to be performed after a processor runs to make the output available and compatible with other Key4hep components. The conversion in both directions includes conversion of the metadata of the collections.

k4MarlinWrapper has been successfully used in different use cases. It runs the complete CLIC reconstruction, with all the combinations of LCIO and EDM4hep inputs and outputs, using the converters. It runs the LCFI+ algorithm for vertex and jet finding, and flavour tagging with the help of the EDM converters. The k4MarlinWrapper enabled the integration of the CLUE algorithm from CMS to replace the usual clustering algorithm in CLIC reconstruction. Contributions such as bug fixes, enhancements and new features were added to several packages to integrate k4MarlinWrapper for different use cases: podio, EDM4hep, various Marlin processors, k4FWCore, k4LCIOReader, k4CLUE, k4SimGeant4 and DD4hep.

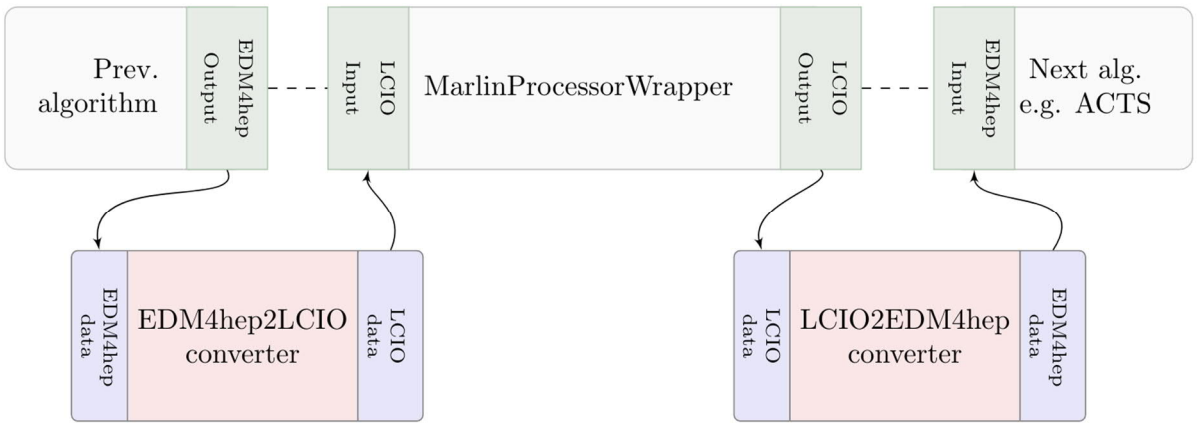

Figure 1. k4MarlinWrapper converters used between algorithms and with different input and output EDM formats.

2.2 Faster Simulation

In 2021 the Faster Simulation task made substantial progress on the application of machine-learning (ML) techniques for fast simulation.

ML inference was integrated into the Geant4 framework. To demonstrate how to perform the inference from a C++ application, example Par04 [9] was implemented and is now distributed with Geant4 release 11.0. The example presents a calorimeter simulation in a simplified geometry. Two ML libraries are available at the moment: ONNX Runtime [10] and LWTNN [11]. Studies of the memory footprint with both libraries indicate a far better performance of inference using the ONNX runtime, as shown in Table 1, which is consistent with the findings of other groups working for the LHC experiments. From the presentations and discussions during the LPCC Fast Detector Simulation workshop [12] it was clear that ONNX Runtime is the most popular inference library.

Table 1 - Comparison between inference libraries LWTNN and ONNX in terms of supported Machine learning libraries, the supported deep learning architecture layers and activation functions, file format and the inference memory footprint.

	LWTNN	ONNX
Supported ML	Saves only Keras models	Saves models from almost all libraries
Suported Layers	All except: CNN, Repeat Vector, Reshape	All
Supported Activation Functions	All except: Selu, PRelu	All
File Format	JSON	ONNX
Resident Memory	4GB	61MB
Virtual Memory	4GB	52MB

Full simulation data was produced to train a variational autoencoder model (VAE), using the Par04 example. This data was published as open access [13].

This data was then used to demonstrate the benefits of meta-learning [14], which can generalise the machine-learning model to adapt to different energies and incident angles, for different calorimeter layouts. The meta-learning based approach allows the model to learn different detector layouts, using the initial parameters from the trained model, combined with a fast adaptation step to tune to the new layout. For example, a model based on sampling calorimeters used in the training sets was adapted to a homogeneous calorimeter. This adaptation takes around 20s for 400 steps, leading to an accuracy of better than 1% in the longitudinal shower profile, as can be seen in Figure 2. This is a huge improvement over the traditional training approach, without prior knowledge, which takes 1200 seconds for the same number of iterations, with far poorer performance; it takes 3 hours (using 10 times more iterations) to approach a similar performance. Meta-learning may prove to be very valuable, especially for the detector studies for future accelerators, where detector parameters are being optimised.

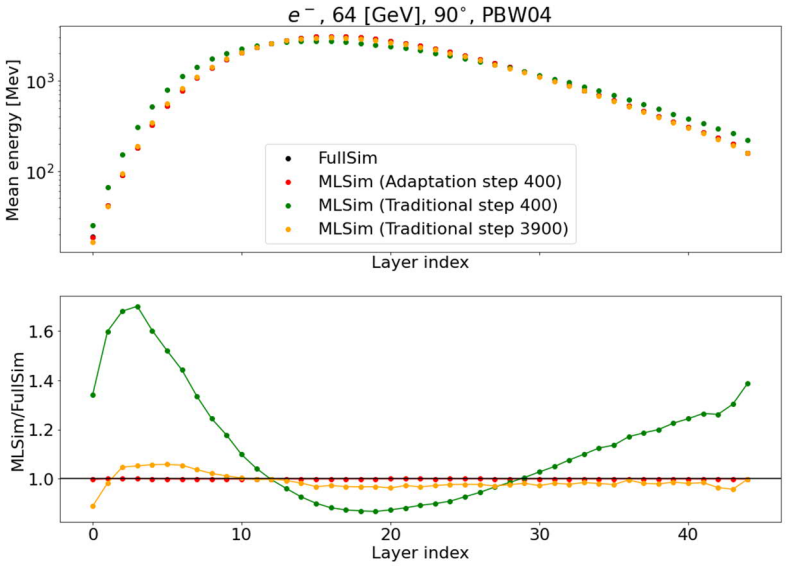

Figure 2: Longitudinal profile for 64 GeV electrons with an incident angle of 90° showing the difference between the fast adaptation and the traditional training using the same number of steps (400) and 3900 steps for the traditional training for better model convergence.

Optimization of the model's hyperparameter space was studied in the context of a summer student project (Poliana Ferreira). Automatic Machine Learning (AutoML) was explored and demonstrated to outperform hand-tuned hyperparameters optimization [15].

2.3 Reconstruction: Calorimetry

During 2021, the EP R&D calorimetry activity focusing on reconstruction with high pileup continued to take advantage of the software experience gained in the context of the new High-Granularity calorimeter (HGCAL) for the forward region for the CMS Phase-2 upgrade [16, 17].

The first step was to integrate the CLUE (CLUstering of Energy) algorithm [18] into the 'Turnkey Software Stack' (Key4hep) thus adapting it to be used in other future experiments featuring high granularity calorimeters. The second step is that a novel algorithm, called CLUE3D [Publication 18], has been developed in the TICL (The Iterative CLustering) framework in the CMS software stack as a possible pattern recognition algorithm to build 3-dimensional clusters, so-called tracksters, which should correspond to different final showers [17].

k4CLUE: CLUE in Key4hep

CLUE is a fast and innovative density-based clustering algorithm to group digitised energy deposits (hits) left by a particle traversing the active sensors of the calorimeter in clusters with a well-defined seed hit [17]. Outliers, i.e., hits which do not belong to any clusters, are also identified. Its performance has been evaluated in CMS (Figure 3).

In order to test CLUE's capabilities for future experiments, the algorithm was adapted by EP R&D to run in the Key4hep stack: it was integrated in the Gaudi software framework and it now supports EDM4hep as a data format for inputs and outputs. The new dedicated package is called k4CLUE [19].

k4CLUE was successfully run as part of the CLIC reconstruction chain, thanks to the synergy of the EP R&D group (Figure 4). The CLIC electromagnetic calorimeter is foreseen as a sampling calorimeter with high granularity and is thus particularly well-suited to test this clustering algorithm. In order to run k4CLUE on CLIC electromagnetic hits, the latest developments in the k4MarlinWrapper were needed. Validation of the EDM4hep clusters produced as output by k4CLUE and comparison with the default CLIC clusters is currently on-going and final physics performance will be determined as part of the 2022 work programme.

CLUE3D

The CLUE3D algorithm is based on the same main features of CLUE, such as the fixed-grid data structure and the basic definition of local density, but it was developed as an alternative pattern recognition algorithm to build tracksters in CMSSW. It clusters 2D Layer Clusters from different layers in 3 dimensions, using their (z, η, ϕ) space positions. Figure 5 shows a clear improvement for reconstructed showers of unconverted photons at lower energies, compared to the default pattern recognition algorithm used in TICL. Its potential for electromagnetic showers will be further explored in 2022.

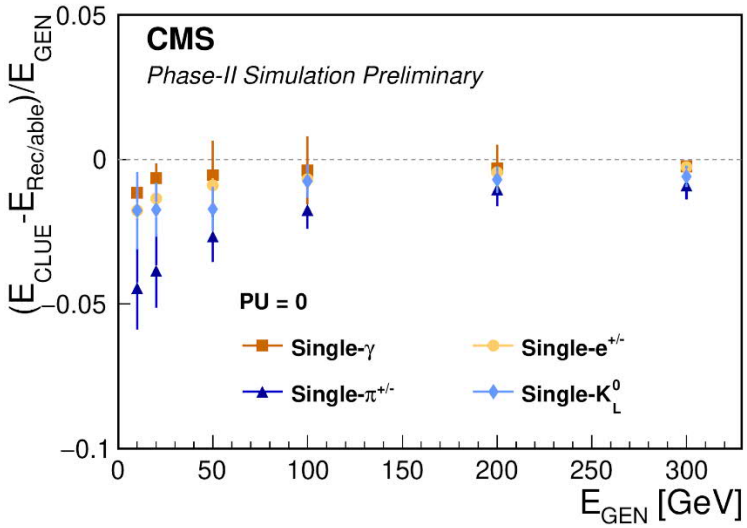

Figure 3: Difference between energy responses before ($E_{Rec/able}$) and after (E_{CLUE}) the 2D-layer hits clustering obtained with the CLUE algorithm. Single photons (orange squares), electrons (yellow circles), pions (dark blue triangles) and kaons long (light blue rhombus) are generated flat between 1.7 < η < 2.7. All samples are without superimposed pileup.

Figure 4: Schematics of k4CLUE input and output interfaced with the default CLIC reconstruction chain.

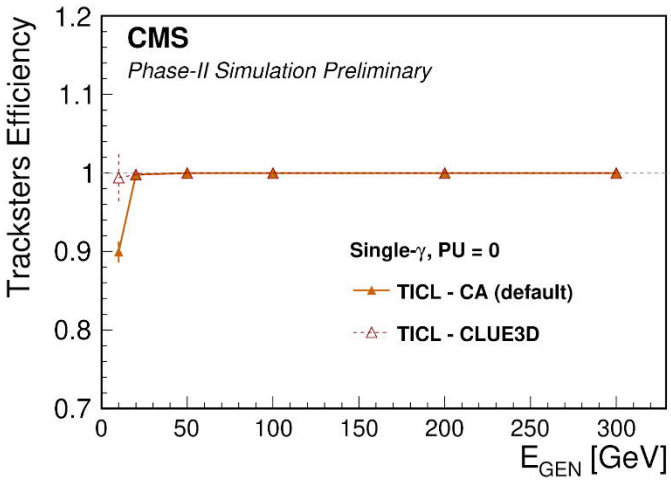

Figure 5: Tracksters efficiency as a function of the generated energy for electromagnetic showers of single photon (orange triangles) events simulated in front of the HGCAL detectors. The default TICL configuration (full markers) is compared to the CLUE3D pattern recognition algorithm (empty markers).

2.4 Reconstruction: Tracking

The tracking developments supported by EP R&D are part of the ACTS project [Publication 19]. ACTS aims to be an experiment-independent toolkit of components for track reconstruction. The project develops a "core" package that is modelled after the (CPU-based) software approaches to tracking that have been successfully used by LHC experiments until now. The project also has more exploratory R&D lines: on machine learning and on algorithms executed in parallel by means of hardware accelerators, like GPUs.

EP R&D supports core development in the ACTS project and coordination work in the R&D. As part of this work, the suite of tracking chain examples has been transformed from a loose collection of executables to a far more sustainable Python library. This example suite is the primary entry point for new contributors to the project and serves as the backbone for many R&D studies and developments targeting the software. This transition has also allowed a strengthening of the automated monitoring of the software, where changes to any monitored output can now be robustly detected and investigated.

A big fraction of the algorithmic code found in ACTS is on trajectory fitting. Implemented on top of ACTS's numerical integration solution, this use case is currently covered by a Kalman Filter. EP R&D support has improved the Kalman Filter implementation to not only be more efficient, but also to reduce the resource consumption at build-time, as shown in Figure 6. This quantity has had to be carefully managed due to the code architecture and heavy use of sophisticated C++ language features. Developments of other approaches to fitting have also seen strong developments in 2021, to a large degree driven by external contributors with support from the core maintainers. This indicates a multiplying effect of direct support of the project by EP R&D, benefitting the project and overall research goals.

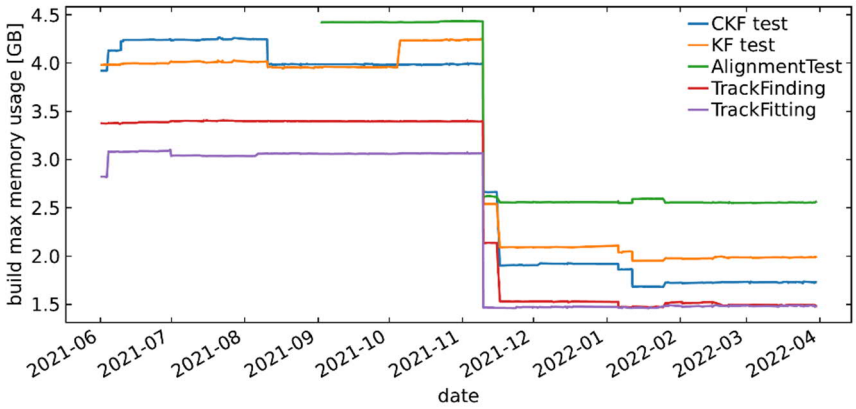

Figure 6: Memory consumption of different ACTS builds over time. The sharp drop is due to dedicated optimization of build resource consumption, which benefits all the built applications.

ACTS is being integrated into the Key4hep stack. Seamless integration between the DD4hep geometry library and ACTS, in order to build the in-memory detector description is crucial for this. To this end, a closer collaborative exchange with the DD4hep developers has been initiated, and work to integrate the ACTS event data model with the EDM4hep package has been started. A viable integration into the stack is targeted for completion in 2022.

On the R&D lines of the ACTS project, EP R&D coordinates the parallelization developments, primarily targeting track reconstruction on GPU hardware. This area comprises vecmem, a library for ergonomic and consistent memory management for different processor types (CPU, GPU, etc.); a surface-based geometry library called detray to support navigation for particle propagation on GPUs, a library abstracting a number of linear algebra backends; and a higher-level library, traccc, tying all three together into a tracking chain. While vecmem and detray are developed currently for ACTS use, they are, in principle, generic and discussions on using them in different projects, e.g., the AdePT R&D for particle tracking on GPUs [20], has begun. In 2021, vecmem has approached stable quality, and started to be used by the other components of the parallelization line. Detray has seen extensive developments and can now support navigation on GPUs. The higher-level suite of algorithms now features implementations of the chain from clustering through seeding and up to track parameter estimation for various technologies. As the assembly of a complete chain including track finding and fitting now seems possible with the foundational pieces of infrastructure, this is one of the primary goals for 2022.

2.5 Efficient Analysis

The R&D activity on efficient analysis software is embedded into the reengineering efforts of the ROOT I/O subsystem for HEP event data storage. The EP R&D programme supports development of the ROOT RNTuple I/O system, which is the designated successor of the current state-of-the-art ROOT TTree I/O. The RNTuple I/O system is designed to match the expected HL-LHC data rates, as well as modern and upcoming I/O hardware.

In 2021, a comparative performance study was conducted and published that underpins the expected performance benefits of the RNTuple I/O stack for typical HEP analysis tasks [Publication 25]. The study compares the RNTuple I/O system to Apache Parquet, which is a popular I/O stack used in the Big Data industry, and to HDF5, which is the de facto I/O standard for High-Performance Computing (HPC) applications (such as weather forecasting or computational biology). Figure 7 shows the end-to-end throughput (compressed data to histograms) for two analyses using typical LHCb and CMS input datasets. Input data is either served from a local fast storage device (SSD) or from remote storage through a network file system (Ceph-FS). In all cases, RNTuple provides significantly faster event throughput than all the competitors, including ROOT's current production TTree I/O. Moreover, the study shows that the TTree I/O is already in some cases outperformed by alternative tools. Both TTree

and RNTuple offer unique features that are critical in the HEP domain such as support for rich event data models, vertical and horizontal data combinations, schema evolution, and support for Grid data storage systems. Figure 8 shows that RNTuple provides the best data compression efficiency of the different I/O systems and their binary file formats. Smaller file sizes directly translate into resource savings in WLCG data storage systems.

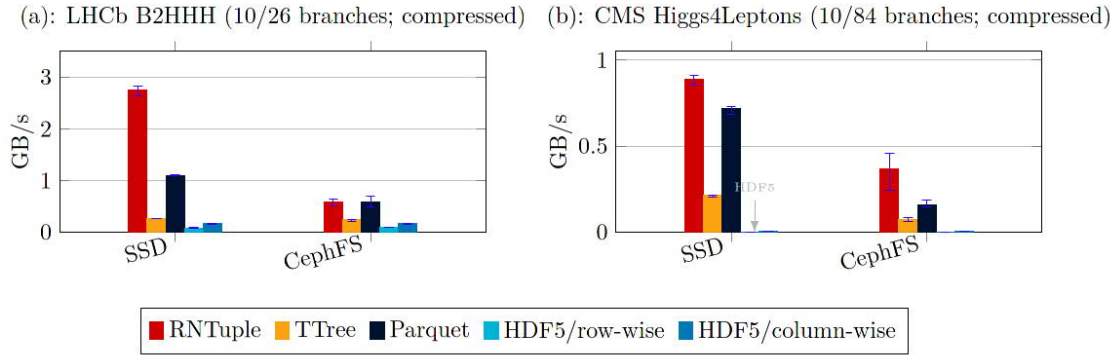

Figure 7: End-to-end throughput of typical analysis code using LHCb and CMS datasets.

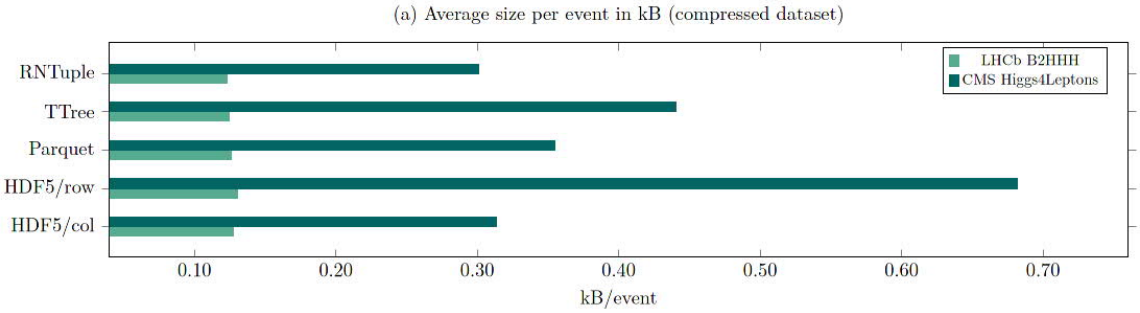

Figure 8: Event size comparison of different file formats (default compression).

The efforts on object store support in RNTuple—performed in collaboration with CERN openlab, Intel, and HPE—resulted in a limited-functionality implementation allowing RNTuple data to be stored in the Intel DAOS object store [21]. Object stores are scalable, file-less storage systems; they became the de facto standard in commercial clouds and are gaining increasing popularity on HPC systems. The RNTuple DAOS backend demonstrated a close-to-target performance of several GB/s end-to-end throughput for typical analysis tasks. Lacking a well-defined standard for object stores, the upcoming years will see continued effort to improve the RNTuple support for the different popular object store choices, such as Amazon S3.

Regarding the integration of RNTuple with existing software stacks, the EP R&D analysis task coordinated a US IRIS-HEP funded project on adding RNTuple support to the CMS core software framework (CMSSW). As a result, CMSSW is now able to produce nano-AODs (event data prepared for analysis groups) in the RNTuple format. This is the first integration of the RNTuple software stack in an LHC experiment software framework.

As a result of an EP R&D supported PhD studentship, a first prototype of the "ROOT Distributed RDataFrame" (Distributed RDF) system was released in 2021. Following the PROOF system from the early 2000s, which is not actively developed anymore, this is the first ROOT-integrated framework to support interactive analysis tasks on computer clusters. While benefiting from the PROOF experience, distributed RDF is based on modern Big Data technologies and aims at exploiting upcoming analysis facilities that are under discussion, e.g., at CERN. The scalability of the prototype has been demonstrated by running physics analysis examples on a HPC cluster at CERN, reaching more than 80

GB/s of real processing throughput on 2048 cores, with different execution engines (see Figure 9). A similar analysis was also carried out with distributed RDF reading data from a DAOS cluster (thanks to the RNTuple backend). In this case, it was possible to use up to 70% of the theoretical bandwidth of the cluster.

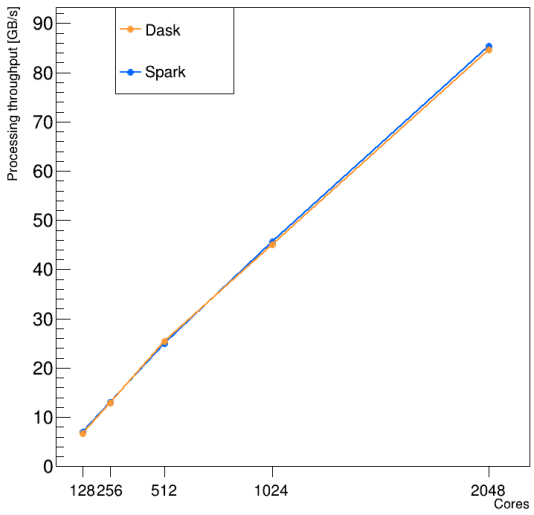

Figure 9: Processing throughput speedup of the Dimuon benchmark with distributed RDataFrame, comparing two different execution engines.

3. Publications and contributions to conferences and workshops

Publications and Conference Proceedings

1. V. Volkl, Status of the key4hep Software Development, presented at IAS Program on High Energy Physics, January 2021, https://indico.cern.ch/event/971970/contributions/4172127
2. V. Volkl, Key4hep: Progress on Common Software, presented at LCWS 2021, March 2021, https://indico.cern.ch/event/995633/contributions/4259672/
3. P. Fernandez Declara, Integrating iLCSoft into Key4hep, presented at LCWS 2021, March 2021, https://indico.cern.ch/event/995633/contributions/4259673/
4. A. Sailer, Key4hep: The Turnkey Software Stack, presented at Software & Computing Round Table, May 2021, https://indico.jlab.org/event/420/#day-2021-05-04
5. P. Fernandez Declara et al., Key4hep: Status and Plans, presented at vCHEP 2021, May 2021, https://indico.cern.ch/event/948465/contributions/4324168/, EPJ Web of Conferences 251, 03025 (2021), https://doi.org/10.1051/epjconf/202125103025
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8. P. Fernandez Declara, The Key4hep turnkey software stack for future colliders, presented at EPS-HEP 2021, July 2021 Proceedings: https://pos.sissa.it/398/844/pdf
9. P. Fernandez Declara, A common software for future colliders: The Key4hep turnkey software stack, presented at ILCX2021, October 2021, https://agenda.linearcollider.org/event/9211/contributions/49387/
10. A. Sailer, Status and Plan of Key4hep, presented at CEPC Workshop, November 2021, https://indico.ihep.ac.cn/event/14938/
11. V. Volkl, Software for detector concepts developments, presented at FCC Higgs/EW WS, November 2021, https://indico.in2p3.fr/event/22887/contributions/102283/

12. P. Fernandez Declara, Key4hep software Stack for Detector Studies, presented at ACAT 2021, December 2021, https://indico.cern.ch/event/855454/contributions/4604989/, proceedings forthcoming
13. D. Salamani, Multi-detector geometry modelling and Geant4 Integration, presented at ML4Jets, July 2021, https://indico.cern.ch/event/980214/contributions/4413578/
14. D. Salamani, Machine Learning for Simulation in High Energy Physics, presented at AIME21, November 2021, https://indico.kfki.hu/event/1331/contributions/2978/
15. D. Salamani et al., Meta-learning for multiple detector geometry modeling, presented at ACAT 2021, December 2021, https://indico.cern.ch/event/855454/contributions/4596400/, proceedings forthcoming
16. LPCC Fast Detector Simulation Workshop https://indico.cern.ch/event/1087522/timetable/
17. E. Brondolin, Novel reconstruction algorithms for an imaging calorimeter for HL-LHC, presented at LCWS 2021, https://indico.cern.ch/event/995633/contributions/4259682/
18. E. Brondolin, CLUE: a clustering algorithm for current and future experiments, poster presented at ACAT 2021, https://indico.cern.ch/event/855454/contributions/4596547/, Proceedings forthcoming
19. A Common Tracking Software Project, https://arxiv.org/abs/2106.13593, accepted by CSBS
20. J. Niermann et al. detray - A compile-time polymorphic tracking geometry description, presented at ACAT 2021, December 2021, https://indico.cern.ch/event/855454/contributions/4605075/
21. P. Gessinger et al., Managing Heterogeneous Device Memory using C++17 Memory Resources, presented at ACAT 2021, https://indico.cern.ch/event/855454/contributions/4605054/
22. P. Gessinger, The Open Data Detector - Tracking and Vertexing, presented at ACAT 2021, https://indico.cern.ch/event/855454/contributions/4596738/
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[21] Intel DAOS (Distributed Asynchronous Object Store). https://github.com/daos-stack/daos/

WP8 Detector Magnet R&D

1. Introduction

Work package WP8 is subdivided in three sub-work packages covering studies in Advanced Magnet Powering for Detector Magnets (WP8.1), the design of a New 4-Tesla General Purpose Magnet Facility for Detector Testing (WP8.4) and studies for Innovation in Magnet Controls, Safety Systems & Instrumentation (WP8.5). Ultra light cryostat studies can be found under WP4 (Task 7.2.2). In 2021, the WP team had one fellow and a technical student, plus a new technical student starting in February, a new Intern from June to November and a new fellow starting in October.

2. Main activities and achievements in 2021

2.1 Advanced magnet powering for detector magnets

2.1.1 ATLAS Toroidal Magnet snubber

Following on the successful testing of the 1/50th scale Snubber demonstrator from 2020, the full Snubber assembly has been designed and realised [1]. The proposed solution to alleviate the large voltage spike and resulting arc is to use the full-scale RC circuit arc suppression snubber with 9.6 F of capacitance as shown in Figure 1.

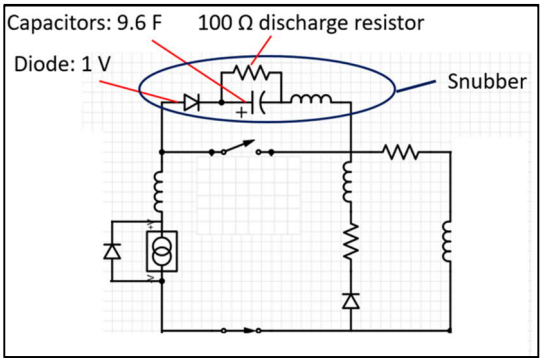

Figure 1 - Schematic showing Snubber inclusion on ATLAS Toroid powering circuit.

After completing various simulations of this full system, supported by the calculation model previously validated with the successful experimental results obtained on a demonstrator, it is expected that the snubber will capture the voltage spike that causes the severe arcing and discharge.

To ensure the viability of using large electrolytic capacitors over the lifetime of ATLAS, endurance testing was completed. This involved rapid charging and discharging cycles of a single capacitor to see if it could avoid degradation for an equivalent of 20 years. These tests showed that after these 200 cycles, zero degradation was noticed and therefore these capacitors were qualified for our purposes as seen in Figure 2. A quality assurance testing campaign was achieved to assess the quality of all the snubber capacitors in use [2].

The final snubber assembly has been fully manufactured and installed in the USA15 cavern directly integrated within the ATLAS Toroid CT2 breaker box as shown in Figure 3. The snubber will be commissioned during the ATLAS Toroid commissioning in early 2022.

2.1.2 Commissioning of the CMS Free Wheel Thyristor system

The Free Wheel Thyristor (FWT) system has been implemented in the underground service cavern at Point 5 on the CMS magnet powering circuit in 2021 to prevent a magnet discharge in case of a disruption on the electrical or cooling networks. This will allow saving time on the magnet availability

for physics data taking. With the FWT, it is now a matter of minutes to have the magnet back to nominal operation (3.8T @ 18 kA), while it was a minimum of 8-hour discharge and ramp-up cycle in the event of a power converter stoppage, as shown in Figure 4. Furthermore, this new powering system reduces the number of magnet cycles caused by unexpected accidents, limiting the risk of degradation, and extending at the same time the magnet lifetime. For the magnet safety, this system still allows the opening of the breakers to safely discharge the magnet. The reconnection of the power convertor was validated during a commissioning campaign, with support from the EP R&D WP8 team. The new safety interlock chains of the magnet safety system were specifically modified and checked by the EP-DT-DI team in charge of controls for superconducting magnets for experiments. This FWT system was developed by CERN SY-EPC group for CMS and successfully commissioned in October 2021. A specific cooling system was designed and implemented by the CERN EN-CV group [3].

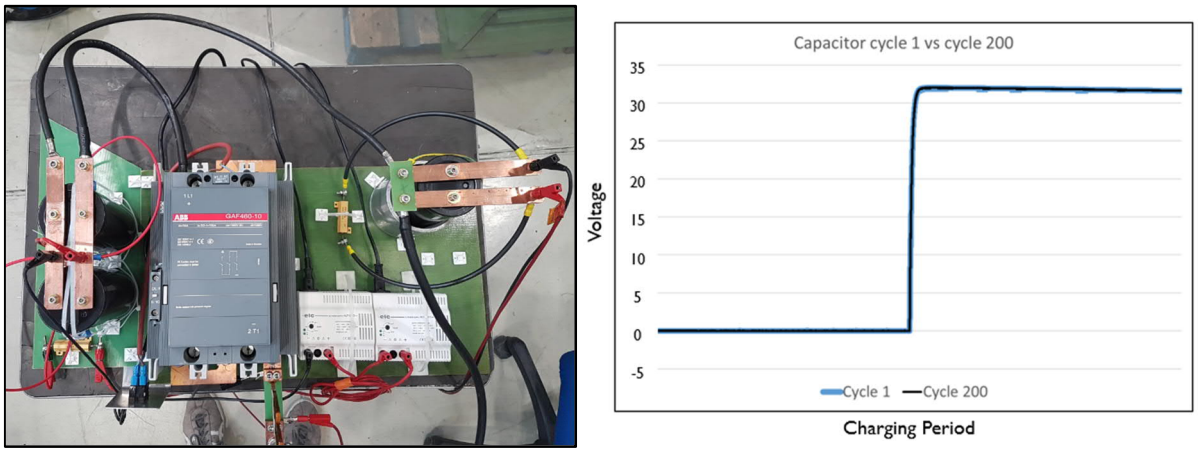

Figure 2 - Capacitor cycle endurance test setup and charge behaviour results of first versus last cycle.

Figure 3 - Snubber installed at the bottom of CT2 ATLAS Toroid breaker box.

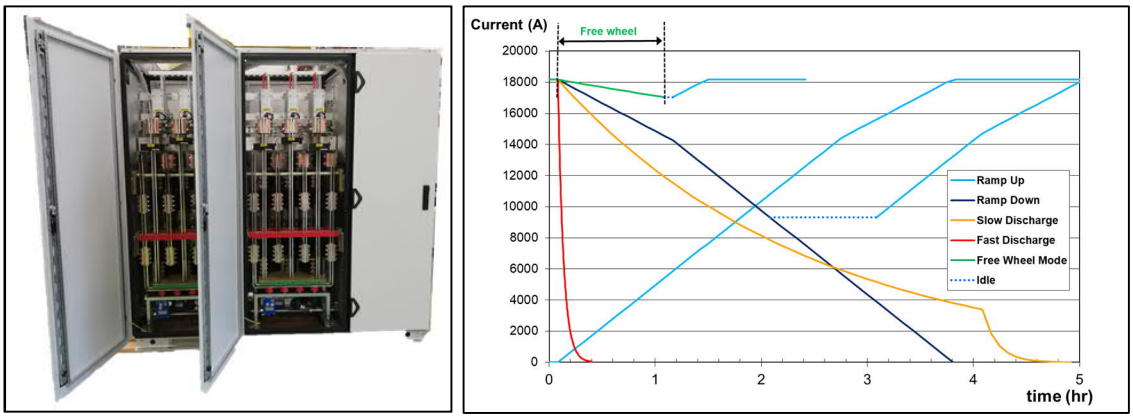

Figure 4 - Thyristor cabinet holding 6 thyristors in parallel and Charge/Discharge scenarios showing effect of FWT.

2.1.3. Study of a persistent mode switch

A persistent mode switch (PMS) in a magnet system would allow for a power supply to be switched off after initial ramping up, leaving the magnet at its nominal field when fully disconnected from the electrical network, which represents a future potential return in energy savings and would contribute to have an excellent field stability without current ripple. Investigations were carried out for a magnet current up to 13kA and a preliminary design was done with a cupro-nickel stabilized filamentary composite NbTi superconductor. The PMS will be built as a coil with a bifilar winding made such to limit the self-inductance as seen in Figure 5. At this stage prototyping of the joints and specific welding investigations have been started to assess the feasibility. Further studies may be continued [3].

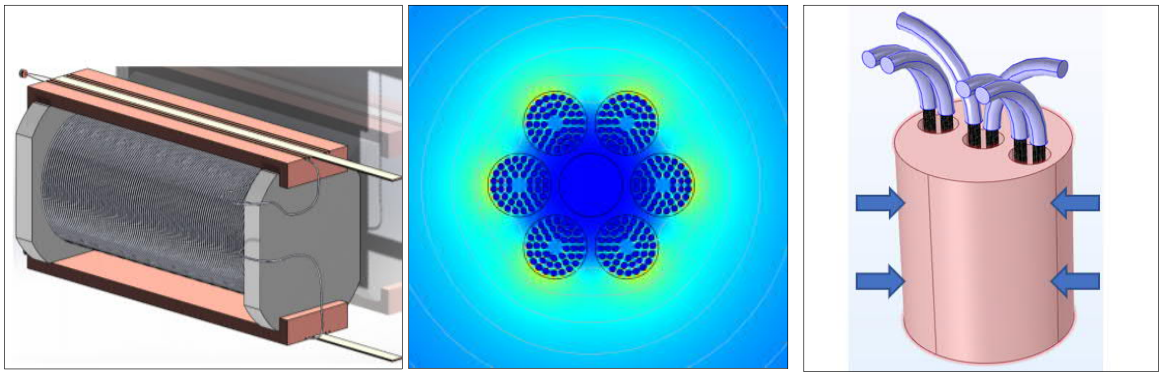

Figure 5 – PMS concept: a coil with six-around-one sub cable geometry and dedicated splice.

2.1.4. High Temperature Superconductor Studies

CERN endeavours using high-temperature superconductors (HTS) in large-scale detector magnet applications, such as superconducting busbar and coil winding applications for the Future Circular Collider detectors, as HTS would permit higher operating temperatures and magnetic field beyond 5 T at 4 K which have been out-of-reach with low-temperature superconductors. The activity has started in October 2021 with the setup of a new test bench to measure HTS critical current. The HTS cable shown in Figure 6 is based on a 4 mm wide REBCO (Rare-Earth Barium Copper Oxide) tape soldered to a copper coated high-purity aluminium stabilizer with outer dimensions of 10 mm × 4 mm. The first results obtained indicate very precise and reproducible characteristics. The experimental study will continue with the measurements of the critical currents of short cable samples with various numbers of stacked HTS tapes in a liquid nitrogen bath at 77 K, verifying the reproducibility of current-to-voltage characteristics and checking if degradation occurs [4].

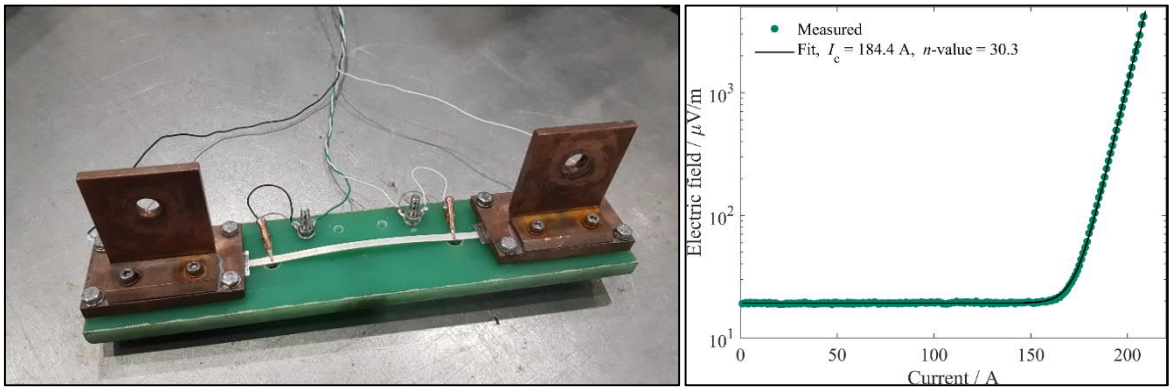

Figure 6 - A short aluminium-stabilized HTS cable sample connected to the critical current measurement setup.

2.2 New 4-T magnet test beam facility

Following on the progress from last year, both Split Solenoid and Saddle type magnet designs have evolved and progressed into the new Split Coil Solenoid and the Magnadon [5].

The aluminium stabilized NbTi superconductor technology is kept as baseline, considering that future detector magnets will be operated below 5 T. High temperature superconductors have been considered in a first approach; they have a good potential as they allow to operate at higher temperature (typ. 20K, 77K) and at higher magnetic field. However, to reach a sound magnet conceptual design more development and engineering work is needed on stability, protection, mechanics and winding techniques [4].

The Split Coil Solenoid (SCS) design has an increased iron shielding and now allows a free bore for solenoidal field in addition to the dipole field, as seen in Figure 7. The increased iron shielding has resulted in a drastic decrease in the stray field at a 5 m distance, reducing from 37 mT to 9 mT. Progress also been made with design concepts of the mechanical support structures to handle the Lorentz forces as seen in Figure 8 [6].

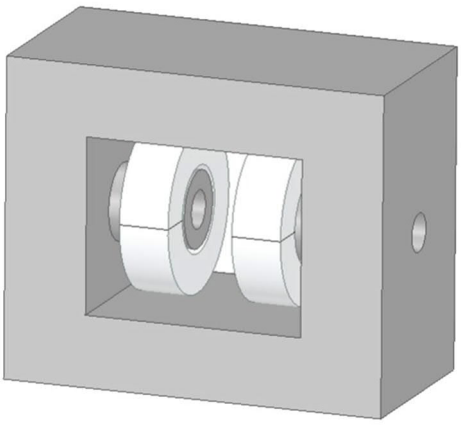

Figure 7 - SCS Coil and tie rod supports.

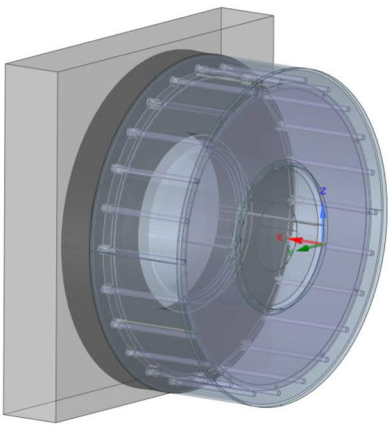

Figure 8 - SCS coil and iron structure.

The Saddle shape coil has been modified into a flared-end tilted racetrack, or “skateboard”, shape and been named The Magnadon (MAGnet for North Area with a Dipole CONcept). This design allows for much lower peak fields within the conductor and incorporates multiple pancake windings of different paths in a stack configuration as seen in Figure 9. Like the saddle design, it still allows the reuse of the

Morpurgo iron yokes. The conductor peak field reduced from 5.9 T to 5.5 T as seen in Table 1. This allowed superconductivity of the NbTi conductor to be maintained with a temperature margin of 2 K. Furthermore, due to the Lorentz bursting forces of 2.5 MN, the design has proceeded to developing the appropriate mechanical support structures as seen in Figure 10 [6].

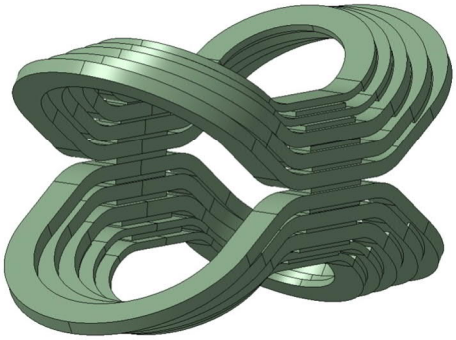

Figure 9 - Magnadon coils.

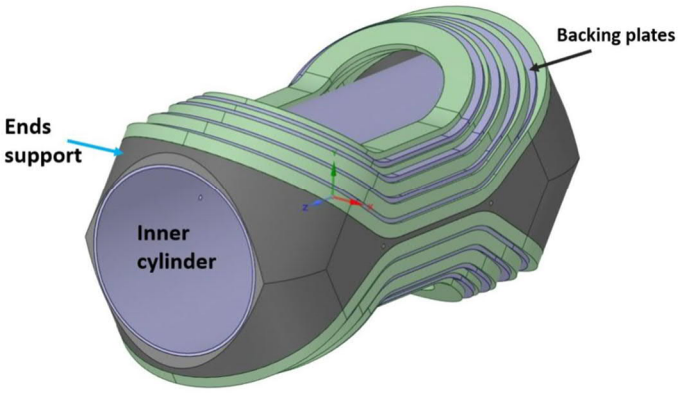

Figure 10 - Magnadon coils and mechanical support structures.

Table 1 - Current 4 Tesla Split Coil Solenoid and the Magnadon specifications.

	Split Coil Solenoid	Magnadon
Field at centre	4T	
Power Supply Current	8 kA	
Free warm for diameter	700 mm	1400 mm
Free warm gap	1000 mm	-
Total stored energy	130 MJ	80 MJ
Peak conductor field	5.68 T	5.5 T
Stray field at 5m	9 mT	11 mT

In addition to the mechanical and electromagnetic designs, thermal computations have been carried out to characterize the indirect cooling of the coils at 4.5 K. Dedicated liquid helium cooling circuits geometries have been designed as seen in Figure 11. A program has been developed for dimensioning the internal cryogenics of these magnets. The software, Thermo-ronika, computes the thermal design parameters for a thermosiphon system.

Based on the results of this software, the SCS has been found to have a pressure drop of 3.6 kPa with a minimum of phase separator height of 3.4 m at a 12 g/s mass flow. The corresponding values for the Magnadon were found to be 2.3 kPa with a minimum height of 3 m also at 12 g/s mass flow [7].

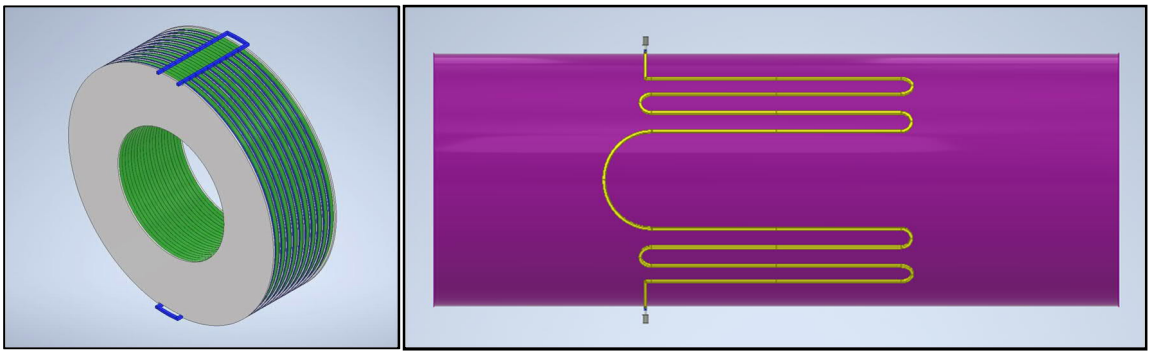

Figure 11 - Parallel branch and serpentine thermosiphons of SCS and Magnadon.

The final free bore and gap dimensions of the two concepts are subject to change based on the evolving needs of the physics user community. Further details of the manufacturing methods and quench behaviour are ongoing. At this stage of the R&D program, it has been proposed to concentrate the efforts on only one magnet conceptual design, that being the SCS. However, based on feedback from the physics user community, the Magnadon may be further explored.

2.3 Cryogenics sample test facility

Following on from the plans of last year, the new cryogenic facility design was finalised, and manufacture and assembly began. A new cryostat will house a 5-T magnet of 200 mm bore for sample testing. The cryostat, platform, support frame with manifold and power distribution have all been completed as seen in Figure 12.

The overall investment is shared with ATLAS magnet group, with significant support from TE Cryolab team (cryostat and magnet tests as well as technical support for P&ID) and EP-DT-DI team providing support for instrumentation and controls. Final tie-ins and commissioning are to take place in 2022.

Figure 12 - New Cryogenic plant location and structures [7].

3. Future works

3.1 Position tracking for magnetic field mapping

Emerging optical technologies in position measurement will be scrutinized for an application in field mapping in view to simplify the B-field mapper's positioning system and increase the versatility of the system. This will be followed up by the EP-DT-TP section of the Detector Technologies group.

3.2 HTS Flux pump

A study has been performed towards the AMS-100 project regarding the development of a HTS flux pump. The developed concept used MOSFET as switches to perform the switching required for the

current ramp up. The next step involves making the flux pump prototypes, investigating optical refrigeration for the HTS switches and investigating other switching methods that do not rely on MOSFETs.

4. Summary

Across the last year, much progress has been made in the context of EP R&D in WP 8. The ATLAS Toroid Snubber has been successfully manufactured, installed and ready for commissioning. The CMS FWT system upgrade has been successfully installed and commissioned. The new 4 Tesla magnet designs have been matured and now detailed studies are continuing to bring the design closer to its final form, which was presented at MT-27 conference in Japan and published in IEEE Transactions on Applied Superconductivity journal. A bespoke thermos-siphon software, *Thermo-ronika*, has been developed. Good progress has been made on the flux pump and high temperature superconductor studies.

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